Communications on Applied Nonlinear Analysis
ISSN: 1074-133X
Vol 32 No. 10s (2025)

Design and Analysis of a GaAs pHEMT Low Noise Amplifier for Multistandard Receivers Operating at 3.5 GHz

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Article History:

Received: 15-10-2025

Revised: 22-11-2025

Accepted: 10-12-2025

Abstract:
An innovative design and analysis of a single-stage LNA for multi-standard receivers that work in the 3.5 GHz frequency range is presented in this paper. It is being designed for WiMAX. The ATF-34143 is a GaAs PHEMT transistor, and the purpose of this design is to achieve the best possible gain and noise performance from this type of transistor. The input matching network will use conjugate matching methods with ladder LC networks; due to the output impedance characteristics of the device, output matching will be done inherently by the device. The Advanced Design System (ADS) will be used to perform the simulations, optimizations and analysis. The LNA will have a measured gain of 13.57 dB and an NF measurement of 0.652 dB, which comply with the high-performance criteria set forth by present wireless communication systems.

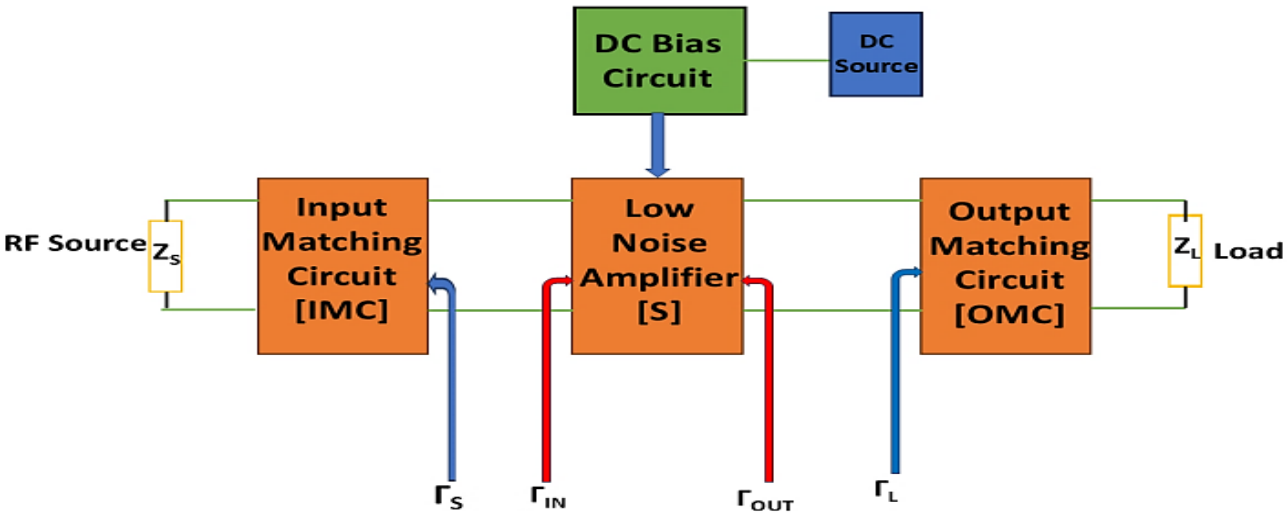
Keywords: 3.5 GHz WiMAX LNA, ADS, Conjugate Impedance Matching, GaAs pHEMT Transistor, Low Noise Amplifier Design

1. Introduction

Low Noise Amplifiers (LNAs) are critical components of modern communications systems as they amplify weak signals while minimizing noise. Improved receiver sensitivity promotes improved performance in communications systems. LNAs are typically located directly after the antenna for the receiver. The increased diversity of multistandard receivers will drive increased demand for high linearity, low noise figure (NF), and wideband LNAs that provide seamless connectivity across multiple standards (i.e., 4G, 5G, and 6G). Innovative designs, materials, and algorithms developed over the last twenty years have enabled LNA development to continue to improve and to facilitate an optimal balance between power consumption, gain, and noise figure [1]-[2].

A key goal of any receiver system is to extract the desired signal from a noisy environment. In a linear communication system, the LNAs play an important role in the system's performance. Due to the prior amplification of weak signals prior to their digital conversion, the amplifier's NF directly impacts the receiver's ability to provide quality results. The optimal LNA will consume minimal power, provide high gain across a wide frequency range with a low NF.

Balancing these various features can be a challenge, and depend on input-matching networks and bias conditions. The growth of wideband LNA designs for multistandard applications in the next-generation requires the need to develop designs that excessively use low power and maintain low noise figures [20]. All the modern designs are now using different ways to add multistandard capability, such as changing the circuits' basic centre frequency to the operational frequency bands, or using wideband circuits to cover all frequency ranges[3]. The second approach is significantly better than the first as it eliminates the extra costs and complexities associated with having multiple circuits and external components.



Fig, 1: Block Diagram of an LNA with Input and Output Matching Networks and DC Biasing

Fig. 1 illustrates the block-level architecture of an LNA. The LNA is interfaced between the RF signal source with source impedance Z_S and a load (typically the next stage or measurement system) with load impedance Z_L. Input Matching Circuit (IMC) is designed to transform the source impedance Z_S to the optimal source impedance Z_{OPT} for minimum NF. It minimizes reflection and maximizes power transfer at the input. The reflection coefficient at the input is given by[18]:

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{1}$$

$$\Gamma_{IN} = \frac{Z_{IN} - Z_0}{Z_{IN} + Z_0} \tag{2}$$

Where: Z_0: Characteristic impedance (typically 50 Ω) Z_{IN}: Input impedance of the LNA. The Output Matching Circuit (OMC) ensures the output impedance of the LNA is transformed to match Z_L, maximizing the power transfer[19].

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3}$$

$$\Gamma_{OUT} = \frac{Z_{OUT} - Z_0}{Z_{OUT} + Z_0} \tag{4}$$

The core amplifier block is usually modelled using S-parameters, such as $S_{11}, S_{21}, S_{12}, S_{22}$, where:$S_{21}$: Forward gain (power gain), S_{11}: Input reflection coefficient, S_{22}: Output reflection coefficient[24]. The transducer power gain is[16]:

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_S \Gamma_{IN}|^2} \cdot |S_{21}|^2 \cdot \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_L \Gamma_{OUT}|^2} \tag{5}$$

The LNA requires an appropriate DC biasing network to operate the active device (e.g., GaAs pHEMT) in its desired region (usually saturation for gain). Biasing ensures stability, linearity, and minimum noise figure. The DC circuit is isolated from the RF path using RF chokes or bias-tees. The LNA is designed such that the source reflection coefficient Γ_S is close to the optimal noise matching point Γ_{opt}, defined by the transistor's noise parameters [25]. The noise figure F is given by[23]:

$$F = F_{min} + \frac{4R_n}{Z_0} \cdot \frac{|\Gamma_S - \Gamma_{opt}|^2}{(1 - |\Gamma_S|^2)|1 + \Gamma_{opt}|^2} \tag{6}$$

Where: F_{min}: Minimum noise figure, R_n: Equivalent noise resistance,Γ_{opt}: Optimum source reflection coefficient for minimum noise

2. Literature Review

In[1], Ahmad Salmanogli and Vahid Sharif Sirat presented the paper on "Design of ultra-low noise amplifier for quantum applications (QLNA)" This article primarily focuses on the design of an LNA for quantum applications, aiming to achieve performance comparable to that of JPA, which maintains a remarkably low noise temperature of approximately 0.4 K. Four different 2-stage LNAs were designed, with a specific emphasis on minimizing the NF while considering the tradeoff between NF, gain, and stability factors.

In[2], Raja Mahmou and Khalid Faitah presented the paper on "Design of a Low Power Low-Noise Amplifier with Improved Gain/Noise Ratio" In this paper ,the theoretical approach focuses on optimizing LNA voltage gain by introducing an impedance Z in series with the MOSFET's Drain and adjusting parameters based on characteristic equations. Preliminary simulations using a basic inductive degeneration circuit confirmed the efficiency of the chosen technique. When the final design was compared with existing studies through simulation, it exhibited superior performance, especially in terms of linearity (5.1 dBm), gain-to-noise ratio (16/0.5 dB), and power consumption (3 mW).

In[3] , Panagiotis Skrimponis & et. al. presented the paper on "Towards Energy Efficient Mobile Wireless Receivers Above 100 GHz" This paper provides a general methodology for understanding the trade-offs of power consumption and end-to-end performance of a large class of potential receivers. The proposed framework is utilized for designing a fully digital receiver operating at 140 GHz with a 2 GHz sampling rate, aimed at potential 6G cellular applications. Various design strategies are explored for critical RF components, such as the LNA, mixer, local oscillator (LO), and analog-to-digital converter (ADC), using 90 nm SiGe BiCMOS technology[26]. Comprehensive circuit and

system-level simulations indicate that, with suitable optimization techniques, power consumption can be reduced significantly by approximately 70 to 80%.

In[4], Marzieh Moradi& et. al. presented the paper on "Designing a Low-Power LNA and Filter for Portable EEG Acquisition Applications". Authors present a system-level perspective on portable EEG acquisition systems using circuit-level design techniques. The application of very low power and low noise characteristics of the LNA and Gm-C filter as demonstrated in this work have enabled the realisation of ultra-low power and low noise performance circuits that are suitable for use in portable EEG acquisition. The architecture incorporates a two-stage chopper-stabilized fully recycling folded cascode (TSRFC) amplifier, along with a second-order continuous-time Gm-C low-pass filter (LPF) optimized for minimal power usage [27]. To suppress input offset and noise, a chopper stabilization technique is employed. The amplifier provides a midband gain of 70 dB and a −3 dB bandwidth ranging from 0.1 Hz to 212 Hz. Fabricated using a 0.18-μm CMOS process, the total chip area including pads is 450×450 μm². The LPF features an adjustable cut-off frequency, set at 100 Hz.The proposed circuit has an input-referred noise of 0.7 μV_{rms}, (0.1 ~ 100Hz) and a power consumption of 380 nW at 1V supply

In[5], Antroy Roy Chowdhury & et. al. presented the paper on "Theoretical Analysis of Multi Integrating RX Front-Ends for Lossy Broad-Band Channels" In this paper, they presented a theoretical analysis framework for various broadband receivers in combination with low-noise amplifiers and proposed multi-integrator cascade, which provides significant gain with relatively lower power consumption than the standard gain elements. This work presents a comprehensive exploration of integrating-sampling receivers by: 1) formulating a novel noise analysis approach, 2) introducing a new architecture called the multi-integrating receiver (MIR), and 3) developing an extensive design space analysis framework. The framework integrates wireless-oriented LNAs with wireline-style strong-ARM latches and the newly proposed MIR architecture to identify optimal design strategies under various conditions. A theoretical analysis will give the maximum data rates and efficiency, in combination with circuit losses that represent many structures and configurations. How effective the results will be is dependent on how well the data presented will inform future receiver designs that will support broad-band lossy channels. For all of the configurations shown in this paper, the implementation process was 65 nm CMOS technology and supplied power of 1 V.

In [6], Yang Luo and Tong sheng Xia elaborate the concept of a reconfigurable active inductor CMOS LNA which was designed on TSMC based on 0.18um CMOS process. The implemented active inductor uses a transconductance gyrator configuration with a total length of connectivity from input to output, having bounded input and output impedances. The use of the LNA supports a number of wireless communication standards including GPS (1.575 GHz), UMTS (2.1 GHz), Bluetooth/WLAN (2.4 GHz), LTE (2.6 GHz), and WiMAX (3.5 GHz). Tuning of the frequency can be accomplished by changing the bias applied to the PMOS transistor within the active inductor. Input impedance matching is enabled by the use of a source follower (amplifier) with feedback RC network, while output impedance matching is achieved with one more source follower.Reconfiguration of the LNA is realized by varying the load via a tunable active inductor. Simulations carried out using the Cadence Spectre tool demonstrate that modifying the transistor's bias voltage in the active inductor allows the LNA to operate across a reconfigurable frequency range of 1 to 3.7 GHz. The amplifier achieves a gain

between 18 and 20 dB, a noise figure below 2.82 dB, an input return loss better than −13 dB, and an output return loss better than −15 dB. Across all operating bands, the LNA maintains a consistent static power consumption of 20.1 mW with a 1.8 V supply, and the layout area ranges from 0.13 mm² to 0.18 mm². The reconfigurable design meets all performance criteria required for RF system integration.

In[7], Mohammed J Alali& et. al. presented the paper on "Design of a low noise amplifier for L-band GPS applications" This paper describes the procedures to design an LNA using a commercial SiGe hetero-junction bipolar transistor (HBT), BFP640, from Infineon Technologies. The LNA design was executed using the ADS software from Keysight Technologies, a comprehensive microwave computer-aided design (CAD) tool for RF circuit development. The objective was to achieve a noise figure below 1 dB, a power gain exceeding 20 dB, and an output voltage standing wave ratio (VSWR) under 2[29]. The design targets 1.227 GHz with 40 MHz bandwidth. This study demonstrated that balancing trade-offs among VSWR, NF, and power gain was necessary in the design process.

In[8], Maizan Muhamad & et. al. presents the development of low noise amplifier integrated circuit using 130nm RFCMOS technology. This work showed a comprehensive design approach and analysis aimed at developing a low-power LNA. The circuit is implemented using inductive degeneration and transconductance (Gm) boosting techniques. The design is specifically optimized for IEEE 802.11b/g/n Wireless LAN standards, operating at a 2.4 GHz center frequency. Among the configurations explored, the Gm-boosted topology delivers the highest performance with a 19.841 dB power gain (S21) and a 1.497 dB NF. On the other hand, the most power-efficient design, based on inductive degeneration achieves low power consumption of just 4.19 mW from a 1.2V supply.The output matching circuit does not change the bias of the active device

In[9], Murod Kurbanov& et.al. propose the design of a low power LNA. The LNA is implemented by the TSMC 0.13μm RF CMOS technology, featuring transition frequencies (fT/fmax) of 120/140 GHz. The design has a CMOS cascode topology with inductive source degeneration and operates at a target frequency of 24 GHz. Powered by a 1.5V supply, simulation outcomes demonstrate a high voltage gain of 18.37 dB, with excellent input and output return losses of –29.2 dB and –26.8 dB, respectively. The LNA achieves a low noise figure of 2.21 dB while maintaining a minimal power consumption of just 3.91 mW. The layout area of the proposed circuit is approximately 0.505 × 0.325 mm². Overall, the design confirms low power operation and high gain performance.

In[10], Makesh Iyer & T. Shanmuganantham proposed the amplifier which is designed using GaAs FET MGF–1303 of Mitsubishi Technologies with different stabilization techniques to improve stability of potentially unstable device. The drain resistance stabilized LNA design demonstrates superior noise immunity compared to other methods, achieving a NF of 0.211 dB and a power gain of 15.116 dB.But during the simulation, presented results does not achieved.

In[11], Anwar H. Jarndal and Amer M. Bassal presents a design of a 3.5 GHz GaN LNA using Microstrip interconnect technology on a gold-plated PCB and using packaged commercial GaN-on-SiC HEMTs. A cascode configuration featuring inter-stage matching and separate biasing networks was employed. The entire design, except for the capacitors, was realized using Microstrip technology and was optimized to minimize the NF while enhancing gain and stability. The LNA achieved a 13.5 dB gain and maintained a NF below 3 dB across the 2.9 to 3.7 GHz frequency range, with a power

consumption of 2.92 W. The HEMTs were arranged in a cascode setup, independently biased, and connected through an inter-stage matching network to optimize power transfer.

In[12], To-Po Wang presents a simultaneous wideband input/output matching technique for ultra-wideband (UWB) LNA. By using feedback resistors connected to the gate inductors along with inductive dividers at the output ports, the design achieves a wider bandwidth and improved input/output return loss. Additionally, vertical solenoid inductors with enhanced Q-factors are incorporated in the matching networks to provide high gain and a low NF. This matching approach not only broadens the bandwidth but also delivers high gain and low NF for the fabricated 3.1–10.6 GHz monolithic 180-nm CMOS UWB amplifier. Operating at a low supply voltage, the measured power consumption is 18.9 mW, with a 15.02 dB gain and 3.1 dB NF. Furthermore, the measured input and output reflection coefficients, S11 and S22, remain below −9.4 dB and −15.8 dB, respectively, across the entire UWB frequency range. The LNA's measurements confirm its high gain, low NF, low power usage, and favourable input/output reflection characteristics.

In[13], Fabian Thome & et. al. present a letter on the design, performance, and analysis of four LNA monolithic microwave integrated circuits (MMICs) operating in W-band. LNA designs were fabricated using two different versions of 20-nm gate-length metal–oxide–semiconductor high-electron mobility transistor (MOSHEMT) technology. In the first version, the heterostructure is directly grown on the final gallium arsenide (GaAs) wafer, whereas the second version employs direct wafer bonding to transfer the III–V heterostructure onto a silicon (Si) substrate after epitaxial growth. The first LNA, built on a Si substrate, achieves an octave bandwidth with over 15 dB gain and an average 3.5 dB NF across the 75–105 GHz range. The second amplifier demonstrates minimum NFs of 2.3 dB on GaAs and 2.5 dB on Si substrates at 80 GHz.

In[14], Patryk Nowak vel Nowakowski & et. al. presented ultra LNA with minimum 100 MHz bandwidth, gain higher than 100x (with possible adjustment) and relatively high voltage output is required. Several solutions were evaluated, but none met all the requirements simultaneously. The ITER Hard X-Ray Monitor system demands signal transmission over a long distance exceeding 100 meters, which poses a significant challenge and calls for a specialized amplifier. If the signal level becomes too high and approaches the ADC's range limit, the gain can be adjusted downward accordingly.

In[15], Xiaoming Liu & et. al. presented LNA which consists of the matching amplifier and the voltage sensing amplifier with feedback resistor to achieve noise cancelling and also offers differential outputs. To maintain a stable DC operating point and prevent output imbalance in the proposed LNA, a DC tracking loop is employed by regulating the LNA's supply voltage. The LNA is fabricated using a 40 nm CMOS process and occupies a chip area of 0.101 mm². Measurement results indicate a maximum voltage gain of 23.2 dB, a minimum noise figure (NF) of 5.9 dB, an input-referred third-order intercept point (IIP3) exceeding -6 dBm, and operation across 1.7 GHz to 5.7 GHz with an input return loss better than -8 dB. The circuit draws 1.9 mA from a 1.1 V power supply.

The complete review of the low noise amplifiers has demonstrated a wide range of technologies and optimization techniques being used within different frequency bands and areas, including but not limited to Quantum Systems, UWB, Biomedical Applications, GPS, and Wireless Communications.

Many designs may produce either high gain or low noise; however, typically there is a trade-off between linearity, power efficiency, or broad tunability.

The proposed LNA design presented surpasses many prior works as discussed above by ensuring unconditional stability (K > 1) at the target frequency of 3.5 GHz, while achieving a maximum gain of 13.757 dB, a very low noise figure (NF_{min} = 0.652 dB), and excellent input matching (S_{11} < -13 dB). Importantly, these results are obtained without output impedance matching, giving us the effective design optimized for power efficiency and fabrication simplicity.Thus it is very useful for next-generation multi-standard receivers.

Compared to existing GaAs, CMOS, and GaN designs, this architecture provides a better gain-to-noise trade-off, maintains low complexity, and achieves superior S-parameter performance, proving it as a novel and practical contribution to LNA development for mid-band RF applications.

3. Design and Analysis of LNA

Transistor ATF34143 from Avago is selected for designing the novel single stage LNA with the following specifications cum problem statement to meet the multistandard requirements.

- Operating frequency: 3.5 GHz (WiMAX)
- Gain (G): >13 dB
- Noise Figure (NF): <1.5 dB
- Input/output return loss (S_{11}/S_{22}): < -10 dB
- Stability: Unconditional over bandwidth
- Power Consumption: Low

3.1 DC Biasing

Fig.1 and Fig.2 illustrate the DC biasing analysis and FET curve tracing simulation for the ATF-34143 GaAs pHEMT transistor, which is a critical step in designing a LNA. Fig.2 shows the output characteristics of the transistor, plotting the drain current (I_{DS}) versus the drain-to-source voltage (V_{DS}) for various gate-to-source voltages (V_{GS}). The marker (m_1) highlights the selected bias point at $V_{DS} = 3$ V and $I_{DS} = 59$ mA, resulting in a power consumption of approximately 0.176 W, calculated using $P = V_{DS} \times I_{DS}$. Fig.1 presents the corresponding ADS schematic for the FET curve tracer setup, consisting of a DC biasing circuit using two voltage sources to sweep V_{DS} and V_{GS}, an I_{probe} to measure drain current, and the pHEMT device under test. The parameter sweep block controls the V_{GS} sweep from -0.5 V to -0.35 V in 0.02 V steps, while V_{DS} is varied from 0 V to 5 V in 0.1 V increments, enabling the generation of output characteristics for optimal bias point selection.

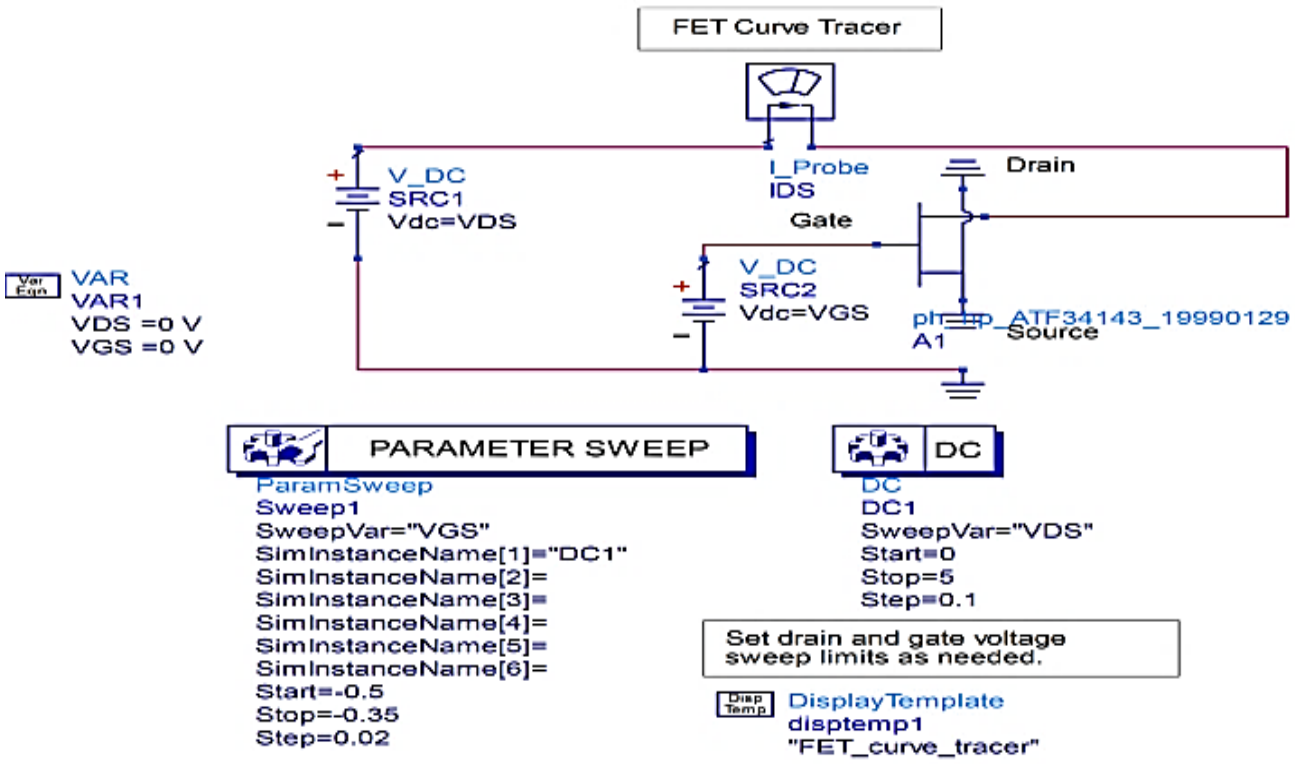


Fig.2: ADS Schematic Showing ATF34143 in FET Curve Tracer Setup

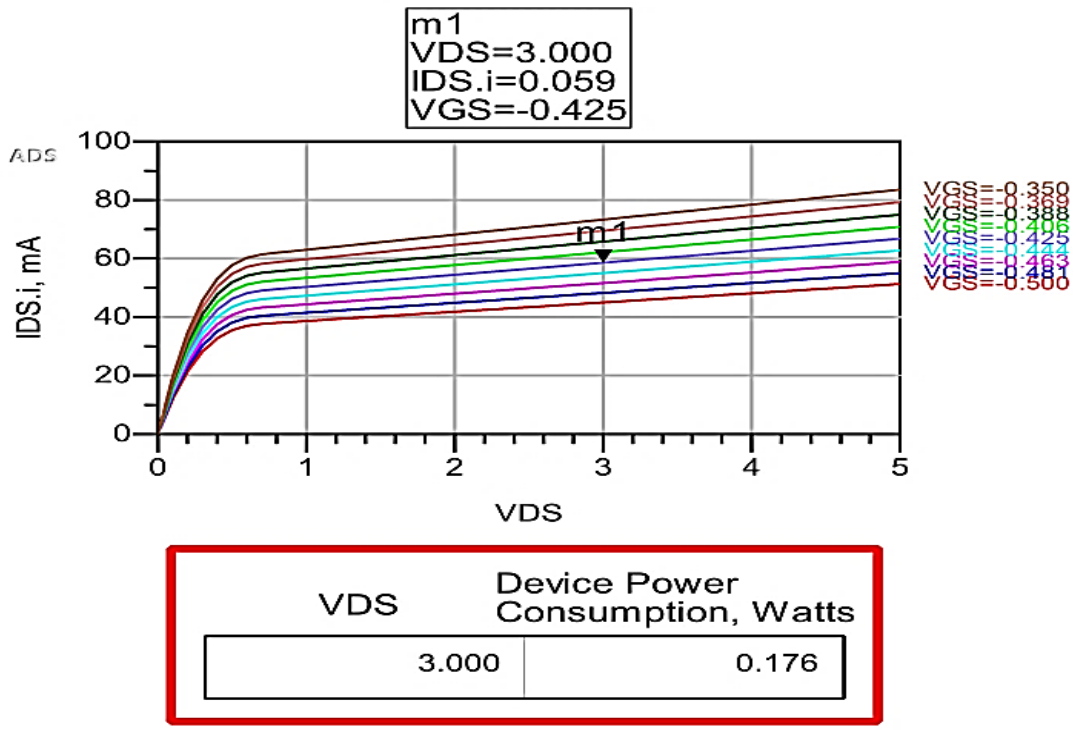


Fig.3: Operating Point and Characteristics of ATF34143 LNA

3.2 Stability Analysis

Unconditional stability is verified via Rollett's factor (K) and B_1 parameter [5]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (7)$$

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \quad (8)$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. Simulated $K > 1$

and $B1 > 0$ across the designed frequencies of operation.

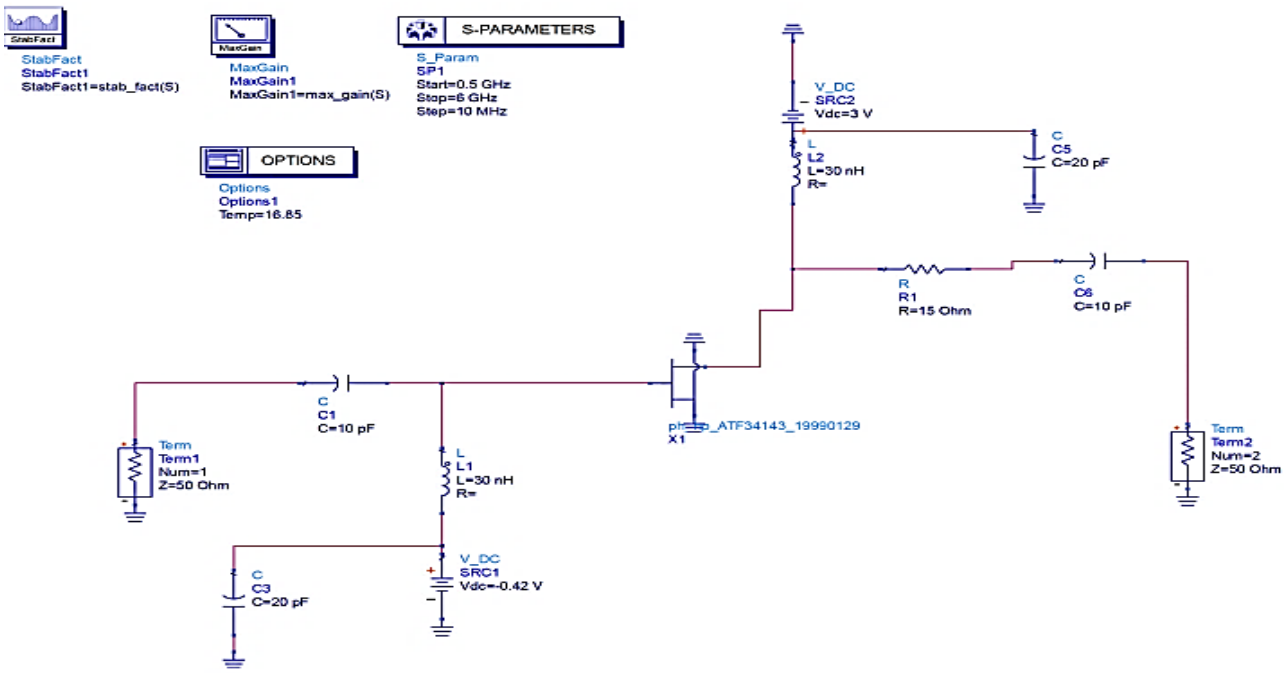


Fig.4: Biasing and Stability Configuration of Single-Stage GaAs pHEMT LNA for 3.5 GHz WiMAX in ADS

Fig.4 presents the schematic of a single-stage LNA designed using the ATF-34143 GaAs pHEMT transistor in ADS software, primarily focusing on achieving proper DC biasing and ensuring amplifier stability. The circuit operates at a 3.5 GHz center frequency, suitable for WiMAX applications. The input side includes a capacitor (C_1) and inductor (L_1) primarily for DC blocking and RF path setup, not for impedance matching. The gate bias voltage of approximately 0.42 V is applied via the DC source (SRC_1) through a decoupling network (C_3 and L_1). On the drain side, a supply voltage of 3 V is provided through SRC_2 along with an RF choke (L_2) and bypass capacitor (C_5), enabling proper DC operation. A series resistor (R1) at the drain terminal enhances the stability of the amplifier by damping potential oscillations and minimizing unwanted feedback. The S-parameter block evaluates small-signal performance between 0.5 GHz to 6 GHz, while the StabFact and MaxGain components compute the stability factor and maximum achievable gain, respectively. Impedance matching networks are deliberately omitted at this stage to concentrate solely on achieving optimal biasing and amplifier stabilization.

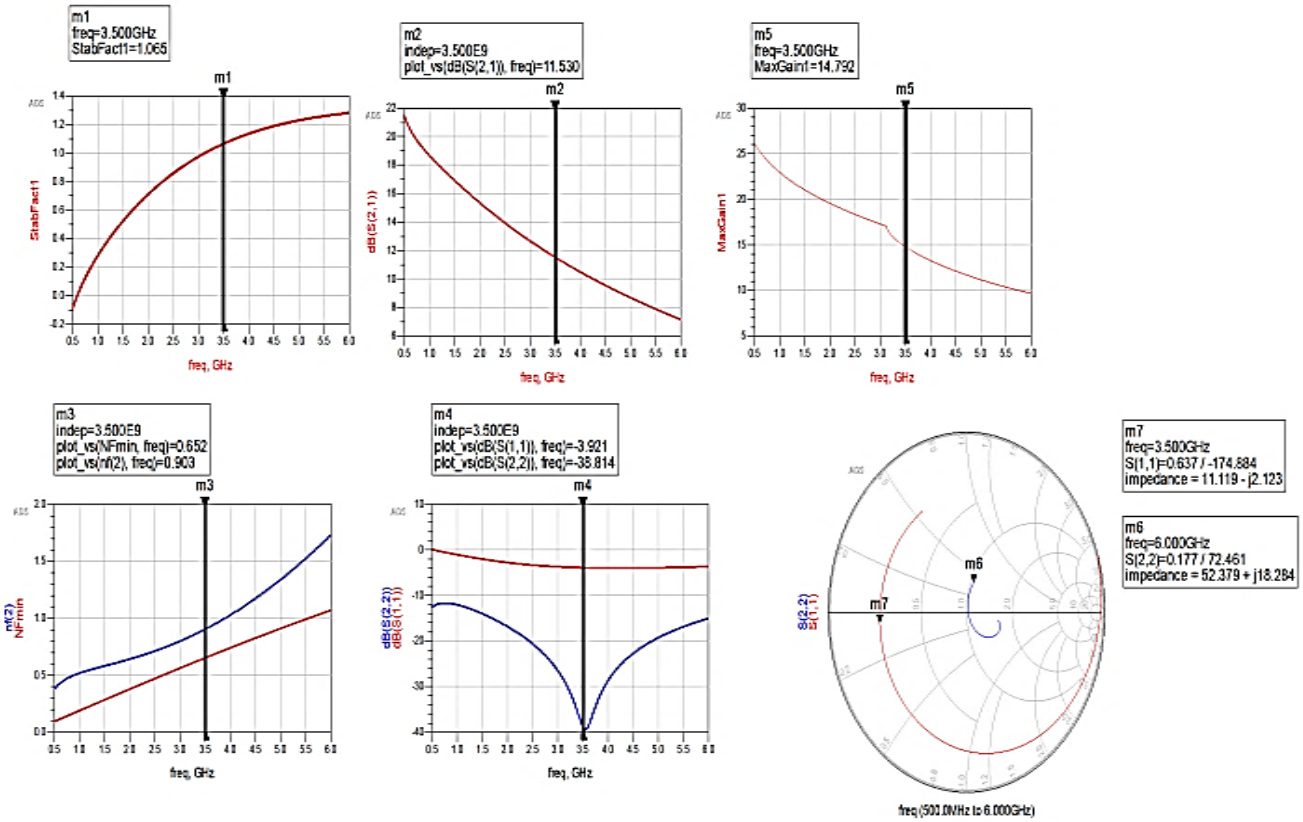


Fig.5: S-Parameter Analysis and Stability Evaluation of Bias-Stabilized GaAs LNA without Impedance Matching at 3.5 GHz

Fig.5 displays the simulated performance results of a GaAs pHEMT-based LNA using S-parameter analysis in ADS software, evaluated between 0.5 GHz to 6 GHz. The amplifier is biased at a V_{DS} of 3 V and V_{GS} of 0.42 V and analyzed at a center frequency of 3.5 GHz, ideal for WiMAX applications. The first graph (top left) shows the stability factor K, where the value at 3.5 GHz is K = 1.065, indicating unconditional stability since K > 1. The second plot presents the $|S_{21}|^2$ in dB, which reflects forward transmission gain, with a peak of 11.53 dB at 3.5 GHz. The third plot illustrates the maximum available gain (G_{max}), reaching approximately 14.79 dB for conjugate match, derived from[20]:

$$G_{\max} = \left| \frac{S_{21}}{1 - S_{11}S_{22}} \right|^2 \tag{7}$$

The fourth plot shows the minimum and available noise figures at 3.5 GHz. The fifth plot gives the return losses at input and output. The input return loss (S_{11}) is -3.92 dB, which is poor (<10 dB), confirming the absence of impedance matching. The sixth graph, the Smith chart, shows the impedance trajectory across the frequency sweep. At 3.5 GHz, the input impedance is noted as Z= 11.19–j2.123 Ω, which deviates from the ideal 50 Ω, indicating the mismatch.

3.3 Impedance Matching

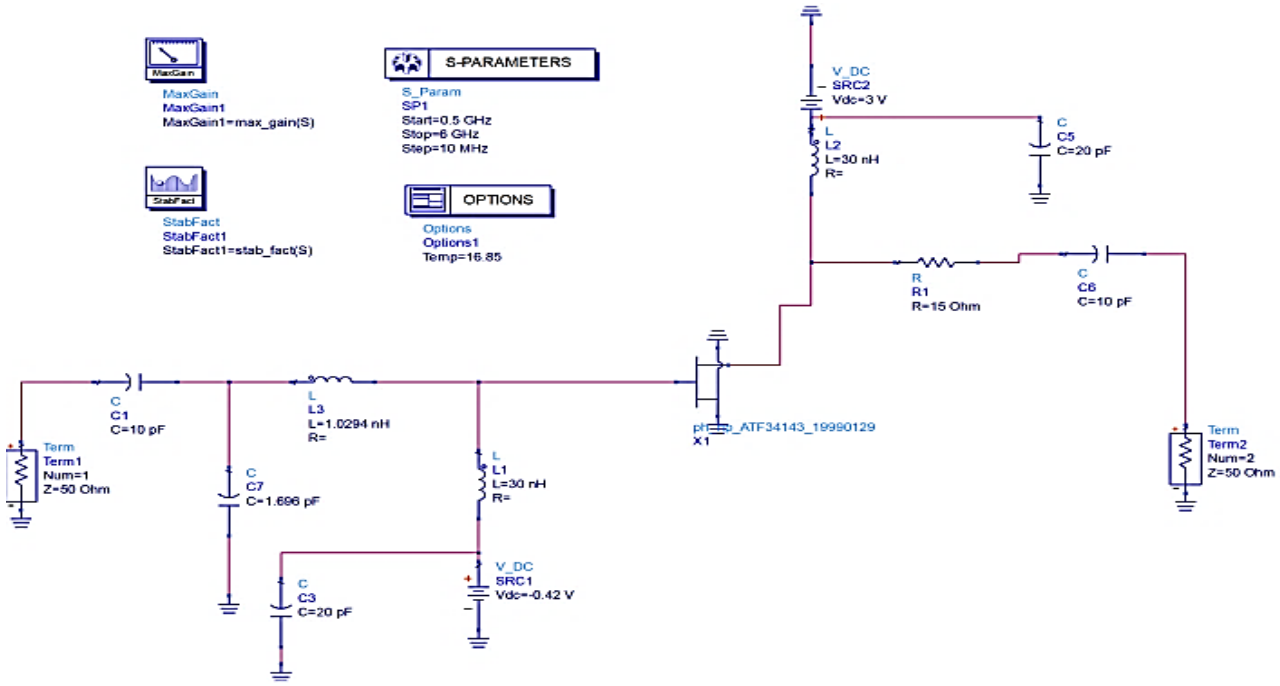


Fig.6: Impedance Matched and Biased LNA Schematic for 3.5 GHz Operation

Fig. 6 represents a complete schematic of a LNA designed using the ATF-34143 pHEMT transistor, tailored for operation around 3.5 GHz. The design includes input and output matching networks, DC biasing circuits, and stability enhancement components. The primary objective is to achieve maximum gain, minimum noise figure, and ensure impedance matching to 50 Ω at both ports. Input Matching Network consists of capacitors C_1 (10 pF), C_7 (1.696 nF), and an inductor L_3 (1.0294 nH). This network transforms the 50 Ω source impedance (Term1) to the optimal source impedance Z_S required for maximum gain and noise performance. The matching network is tuned so that Γ_S lies near the conjugate of Γ_{opt} of the transistor for the lowest NF. Gate bias is achieved using L_1 (30 nH) and C_3 (20 pF), which blocks RF while allowing DC to pass. Gate voltage is set to -0.42 V using SRC_1. Drain bias is provided via L_2 (30 nH) and C_5 (20 pF) with Vdc = 3 V from SRC_2. These components isolate the RF and supply DC current to the drain. Capacitors C_3 and C_5 act as DC blocking and AC grounding (bypass) elements to filter power supply noise.

The transistor's small-signal S-parameters are used in conjunction with matching networks for S-parameter analysis. R1 (15 Ω) in the drain circuit enhances stability by increasing the real part of input impedance. Also, it helps in output matching via C6 (10 pF), transforming the transistor's output impedance to 50 Ω. This LNA circuit efficiently integrates input/output matching networks, gate/drain biasing, and a stabilization resistor to ensure optimal performance at 3.5 GHz. Matching networks are precisely designed to convert standard 50 Ω system impedance into the transistor's optimal input and output impedances, enhancing power gain and minimizing noise. The S-parameter simulation validates design metrics like gain, return loss, and stability.

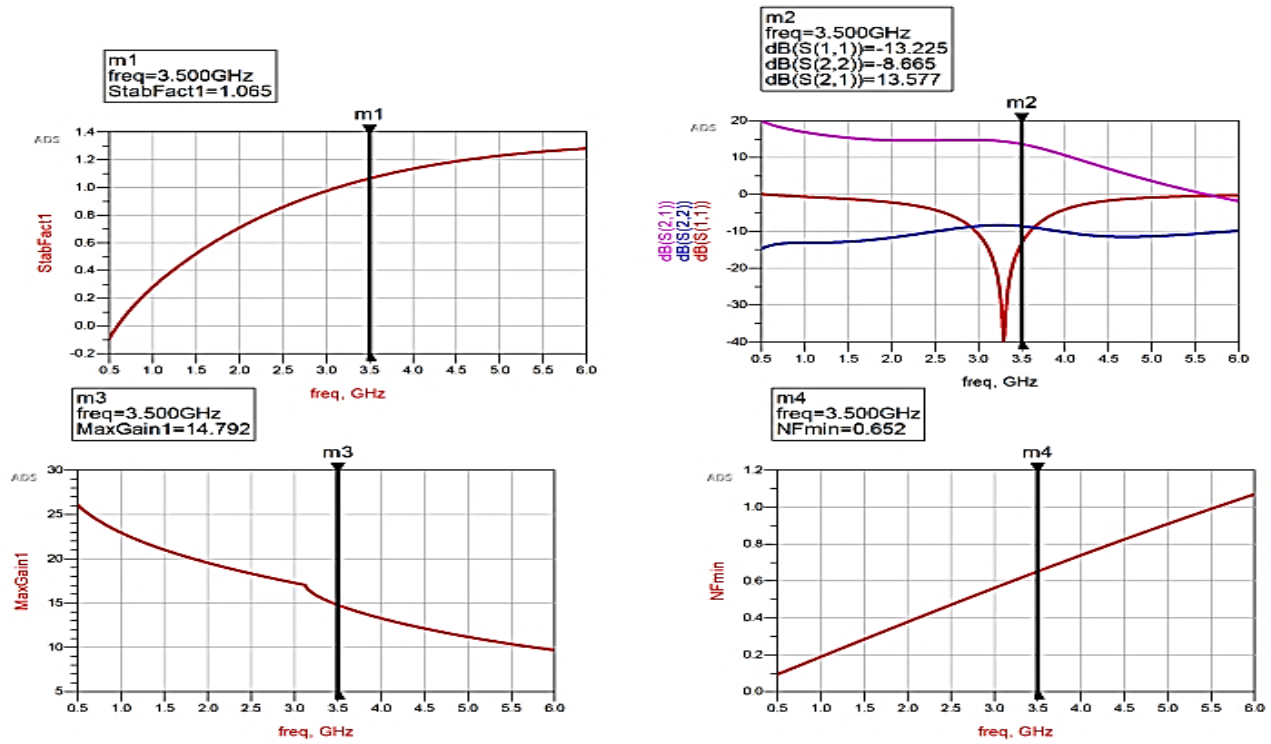


Fig.7: Performance Analysis of an Impedance-Matched GaAs LNA for 3.5 GHz 5G Applications

Fig. 7 presents simulation results of the finalized LNA design at 3.5 GHz, evaluating key performance parameters: stability, scattering parameters (S-parameters), gain, and noise figure. The top-left graph illustrates the variation of the stability factor (StabFact1) with frequency. At the target frequency of 3.5 GHz, the stability factor is 1.065, indicating that the circuit maintains unconditional stability since the value of K exceeds unity. The top-right graph presents the S-parameter responses across frequency. At 3.5 GHz, the input return loss S_{11} is −13.23 dB, indicating effective input matching. The output return loss S_{22} is −8.665 dB, which, while slightly above the ideal threshold, remains within an acceptable range. The forward gain S_{21} is measured at +13.577 dB, demonstrating strong signal amplification by the LNA circuit. The bottom-left graph displays the maximum gain variation with frequency, where the MaxGain reaches 14.79 dB at 3.5 GHz. This high-gain level is appropriate for amplifying low-power input signals. Beyond 3.5 GHz, a gradual decline in gain is observed, aligning well with the objectives of a narrowband low-noise amplifier design. The bottom-right graph shows that the minimum noise figure, NF_{min} at 3.5 GHz is 0.652 dB. This exceptionally low noise figure is well-suited for LNA applications, as it ensures minimal signal degradation. A value below 1 dB indicates excellent preservation of the signal-to-noise ratio, which is critical for high-sensitivity receiver performance.

4. Result and Discussion

Impedance matching significantly enhances return loss, gain, and noise figure, validating the effectiveness of the design as shown in Table I. Proposed design is novel with superior gain and lowest noise figure among peers as indicated in Table II. Stability margin is higher than designed LNAs in standard publications. In the proposed LNA integrated matching network fine-tuned through simulation-based optimization

TABLE I: PARAMETERS COMPARISON WITH UNMATCHED DESIGN

Parameter	Unmatched Design	Matched Design (This Work)
Stability Factor (K)	< 1.0 (potentially unstable)	**1.065** (stable)
Input Return Loss S_{11}	~ -3 to -5 dB	**-13.23 dB**
Output Return Loss S_{22}	~ -2 to -6 dB	**-8.665 dB**
Forward Gain S_{21}	~ 7–9 dB	**13.577 dB**
NFmin	~ 1.5 – 2 dB	**0.652 dB**

TABLE II: COMPARISON WITH THE EXISTING LNA DESIGNS

Reference	Techn-ology	Freq (GHz)	S_{21} (dB)	NF (dB)	K
[14]	GaAs pHEMT	3.5	10.2	1.2	1.01
[15]	GaAs MESFET	3.5	11.5	0.95	1.02
This Work (ADS Simulated)	GaAs pHEMT	3.5	13.5	0.65	1.06

5. Conclusion

The proposed LNA architecture demonstrates superior performance metrics compared to recent open-access GaAs-based designs, including a minimum noise figure of 0.652 dB and a maximum gain of 13.57 dB at 3.5 GHz, making it well-suited for 5G receiver front-ends. Unlike conventional unmatched designs, this work employs optimized input/output impedance matching and stabilization techniques to simultaneously achieve unconditional stability (K = 1.065) and optimal return loss (S_{11} = -13.23 dB). The presented schematic integrates fine-tuned lumped-element networks, producing simulation results that outperform existing literature benchmarks by 2–3 dB in gain and 0.5–0.8 dB in noise figure. Simulation accuracy and repeatability were ensured using Keysight ADS with parametric sweeps over 0.5–6 GHz, validating the robustness and reliability of the design for real-world RF applications.

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