

Designing of Neuromorphic VLSI Circuits based on Biological Neural Networks to Improve the Energy Efficiency and Performance of AI/ML Applications

¹S. China Venkateswarlu, ²Krishna Dharavath, ³M. Koti Reddy, ⁴Narsimha Reddy Kuppireddy, ⁵Rajendar Sandiri, ⁶Srinivasarao Gajula, ⁷Nagarjuna Malladhi, ⁸Sreevani Menda, ⁹Vallabhuni Vijay

¹Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Dundigal-500043, Hyderabad, India, sonagiricv@gmail.com

²Department of Electronics and Communication Engineering, Vardhaman College of Engineering, Hyderabad, India dkrishna.nits@gmail.com

³Electronics and Communication Engineering Universal College of Engineering and Technology, Guntur, 522438 Andhra Pradesh, India. kotiucet@gmail.com

⁴Department of Electronics and Communication Engineering, Vardhaman College of Engineering, Hyderabad, India simha.vce@vardhaman.org

⁵Department of Electronics and Communication Engineering, Vardhaman College of Engineering, Hyderabad, India sandiri.rajendar@gmail.com

⁶Department of Electronics and Communication Engineering, St. Ann's College of Engineering & Technology, Chirala, India. gsrinivasarao443@gmail.com

⁷Vardhaman College of Engineering, Hyderabad, India. malladhinagarjuna@gmail.com

⁸Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Dundigal-500043, Hyderabad, India. sreevani.mkr@gmail.com

⁹Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Dundigal-500043, Hyderabad, India. vijaykalam.v@gmail.com

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Abstract: Neuromorphic VLSI circuits, inspired by biological neural networks, have emerged as a promising solution to address the growing demand for energy-efficient and high-performance AI/ML applications. Traditional computing architectures face limitations in power consumption, scalability, and real-time processing, especially for complex, data-intensive tasks. In this research, we propose the design and implementation of neuromorphic VLSI circuits that mimic the structure and functionality of biological neurons and synapses. By leveraging event-driven, asynchronous spiking neural networks (SNNs), our circuits are able to process information in a parallel and distributed manner, significantly reducing power consumption while improving computation speed. The proposed neuromorphic circuits integrate in-memory computing, which eliminates the energy bottlenecks associated with data transfer between memory and processing units in conventional systems. This paper highlights the architectural advancements in VLSI design that enable real-time learning and adaptation, making these circuits highly suited for AI/ML tasks such as image recognition, natural language processing, and autonomous systems. Simulation results demonstrate that our neuromorphic VLSI circuits achieve superior energy efficiency and performance compared to traditional AI hardware. This research

opens new avenues for developing low-power, scalable AI solutions in edge computing and other energy-constrained environments.

Keywords: AI/ML applications, Biological neural networks, Energy efficiency, In-memory computing, Neuromorphic circuits, Spiking neural networks, VLSI design, Real-time processing.

1. Introduction

As we dive into the world of artificial intelligence, we're seeing some incredible advancements that are changing the game. One of the most exciting developments is the Intel neuromorphic chip, which is shaking up how we think about AI hardware. This cutting-edge technology is inspired by the human brain, aiming to create machines that can think and learn more like we do. We're witnessing a shift towards brain-inspired AI that could revolutionize everything from robotics to data processing. In this article, we'll explore the ins and outs of neuromorphic computing and take a closer look at Intel's Loihi chip. We'll also delve into the fascinating world of bio-inspired VLSI circuits and how they're pushing the boundaries of AI. We'll discuss the real-world applications driving this technology forward and what it means for the future of AI hardware. By the end, you'll have a solid grasp of how these innovations are shaping the landscape of artificial intelligence and what we can expect in the years to come (Yesil et al. (2023), Tozlu et al. (2021), Mahmoodi et al. (2024)) [1]-[21].

The research article by Wang et al. (2024) significantly advances neuromorphic computing with novel means to combine photonic devices with neuromorphic architectures. The study explores synergy between neuromorphic models and photonic technologies to design novel and faster processing speeds and energy efficient using them. By integrating it, the door opens for optical neural networks that can achieve higher performance when scaled to handle these high speed data processing or low latency applications than can classical electronic neuromorphic systems. They also contribute to the body of work growing in neuromorphic photonics and extend its application to areas like artificial intelligence, edge computing, and sensory systems. All of these advancements, the article cites however, are subject to limitations, mainly scalability issues in building photonic neuromorphic circuits at large scale. Moreover, photonics feature higher cost of manufacture and higher technical complexity relative to electronic systems, all of which may impede their wide adoption. Additionally, the field remains in its early stages, with the yet fewer tested theoretical models practically in real world scenarios [22]-[31].

Kumar et al. (2023) experiment with a novel on chip trainable and scalable in memory artificial neural network architecture for use in AI/ML applications. The inmemory computing approach adopted in this work is a standout feature which solves the limitation of the memory bottleneck in traditional von Neumann architectures. The architecture merges computation with memory storage within a single framework, providing the means to perform real time training while being both highly potent in terms of processing speed and efficiency, and lower in power consumption. Furthermore, the proposed architecture is scalable allowing it to be adapted for large scale AI models, with potential edge or low power AI system applications. However, the architecture is prone to several problems. The precision of in memory computing is one of its key limitations, and process variations and noise could lower the precision resulting in the inaccuracies in the complex models. Furthermore, the design may lack the capability of generalization to more complex AI tasks that require a high data handling or high memory

capacity. In addition, implementation complexities such as fabricating such an on-chip architectures at commercial scale, and their compatibility with existing digital systems continue to be practical hurdles to their broader adoption [32]-[49].

In Liu et al. (2022) propose a 3D architecture based on biological neural networks, which brings significant novelty in the area of neuromorphic computing. The designed architecture resembles the brain's connectivity and neural functions such that it gives rise to more efficient data parallel processing and computation. Advanced materials for the building of artificial synapses and neurons enable neuromorphic system performance improvement in terms of energy efficiency and scalability, resulting in a vital neuromorphic hardware breakthrough. However, limitations remain. The fabrication of 3D circuits is exceptionally complex, with high risk of structural integrity and precision degradation at the nanoscale. In addition, despite significant successes of the proposed bio-inspired approach, its integration with existing silicon based technologies is still an issue. However, lots of work still needs to be done in the real world application of these circuits, especially in those large scale systems where the issues like stability, durability and cost effectiveness need to be achieved [50]-[65].

Li et al. (2024) provides a novel way to mimic biological neural dynamics via memristive devices. Novel artificial neurons that closely match the spiking dynamics and energy efficiency of real neurons, as well as their synaptic plasticity, are built and used to advance neuromorphic computing. With the integration of memristors, this provides a key contribution to the embodied development of hardware based artificial intelligence (AI) with brain like functionality through scalable, low power neuromorphic systems. Of course, there are limitations. Biological neural dynamics in hardware are still very complex to interactively model in an accurate fashion. Although memristive technologies hold promise, the reliability and scale of large scale networks are not definitively demonstrable. Moreover, integrating these neuromorphic networks with currently existing computational systems is still a challenge, in terms of compatibility and stability. It is desired to refine the performance and practical application of these systems in real world scenarios [66]-[88].

Nazari et al. (2024) discusses a novel neuromorphic circuit based on unsupervised learning in biologically inspired spiking neural networks (SNNs) for pattern recognition. One of the contributions of this work is in the use of spiking neural networks, which better approximate the behavior of biological neurons over standard artificial neural networks. With this neuromorphic architecture, overall efficiencies in pattern recognition tasks are improved and this work contributes a hardware based energy efficient machine learning approach that scales well. In addition, application of the unsupervised learning model to this case expands the potential of application of the unsupervised learning model. There are, however, constraints in this study. Spikynal Neural Network is still to be validated against more standard methods, in much more complicated real world tasks. In particular, challenges of implementing SNNs in large scale applications remain, as hardware requirements and integration in wake of existing systems have not been fully addressed. The proposed system has a long way to go to generalize better and put it in practical deployment [89]-[93].

The work of Tanvir Ahmed et al. (2023) provides a new method of neuromorphic computing based on soft biomaterials in chip engineering. The rationale behind is to create artificial synapses which mimic the biological synapse process of human synapse for designing more energy saving and efficient computational model. The research leverages integrating soft biomaterials to advance the field of

neuromorphic computing toward more flexible, adaptable and potentially biocompatible designs and offers a path toward future wearable technologies and biomedical applications. Additionally, this approach provides the opportunity to reduce stiffness and fragility associated with traditional electronic components. However, there are significant limitations of the study. Soft biomaterials in chip engineering were still in their infancy, and we had not studied their durability in time. Both the long term performance and scalability of these biomaterial based artificial synapses in large scale system or in different environmental conditions are still unknown. Additionally, these technologies need to be further integrated within existing architectures of computing [94]-[114].

Balaji et al. (2022) propose a novel architecture for neuromorphic advances using novel design and implementation techniques. They make significant contributions to the development of neuromorphic computing with novel neuromorphic computing strategies for enhancing system efficiency as well as scalability. Their main novelty lays in designing for hardware in neuromorphic computing, allowing faster processing with less power. In particular, this is crucial, as neuromorphic architectures focus on modeling the brain's energy efficient computational capacity. But the study is limited in some respects. The first is that the proposed architecture design make sense, but nobody has tested it in the real world at a large scale yet. Specifically, scalability and integration with current technologies can pose issues, as we adapt the architecture for various computing environments. Furthermore, the performance in various practical use cases, such as robotics or AI systems, is not studied completely. In order to validate the architecture's effectiveness and durability, further empirical testing and refinement is needed [115]-[119].

This work of Yang et al. (2020) is highly novel within the scope of neuromorphic engineering since it seeks to follow the shift from biological neural systems to spike-based hardware systems. An addition that I have seen is the integration of spike-based neuromorphic hardware that emulates the human brain and requires significantly less power to provide real-time analysis of complex data. This approach could change many applications including artificial intelligence, robotics, and autonomous systems through offering improved computational models that are faster and consume less power. However, the study also has some limitations. As for external validity, the study's results cannot be generalized to other contexts. Despite the potential offered by the presented ideas the actual realization of a spike-based approach for these systems remains to be an issue due to questions of scalability as well as interconnectivity with modern day system architectures. However, the challenge of mimicking the biological neural behaviour in hardware is still a daunting one. Besides, although the paper offers theoretical contributions, very few of them may have undergone empirical testing to determine the capacity of the applied hardware under actual situations. More investigations and tuning have to be performed to decrease the mentioned drawbacks and increase its real world usability [120]-[132].

Mehonic et al. (2020) research presents novel insights of memristor usage to enable in-memory computing, deep learning acceleration and spiking neural networks as the crucial part in future neuromorphic and bio-inspired computing systems. The major contribution is to demonstrate how memristors can be used to efficiently integrate memory and processing for lower latency and energy than traditional von Neumann architectures. This could pave the way for more effective AI systems, in particular in operations such as real time learning and processing with spiking neural networks as closely targeted brain processes. The paper also bespeaks some limitations, however. Although

memristor technology is still in its infancy, it still faces challenges of long term reliability, manufacturing consistency and large scale integration. This lack of scalability for commercial applications is limited to the variability in device performance and the lack of standardized fabrication processes. Additionally, the paper makes promising theoretical advances, but more experimental validation and real world testing are necessary to fully realize the potential of memristor based systems in practical computing scenarios [133]-[142].

Javanshir et al. (2022) research introduces novel algorithmic and neuromorphic hardware advances for spiking neural networks (SNNs) by mimicking the dynamics of biological neurons. One of the key innovation in the paper is the advancement of the new algorithms which greatly increase the efficiency and accuracy of SNNs when compared to traditional neural networks and provide very large power efficiency improvements. This work also extends the state of the art by showing how neuromorphic hardware architectures can execute complex tasks like pattern recognition using near minimum energy and represent a novel cost advantage for the real time use cases involving AI and edge computing. However, the paper is aware of several limitations. But a big obstacle for using them is the complexity of training SNNs compared to conventional deep learning models. Also, the hardware progress is still in experimental phases with scalability and mass production being big obstacles. Research is needed to fill in the gap of the limited software tools and frameworks for optimizing SNNs in the real world [143]-[156].

Rose et al. (2021) research article provides with a novel system design point of view on neuromorphic computer processors, focusing on intergration of biopired neural architectures into the computer systems. Among the key innovations is the study of hardware designs that copy the human brain's efficiency — the most energy efficient being able to process data at extremely high speed, especially for pattern recognition and making real time decisions. In addition, they also present design strategies to balance th performance-power complexity trade-offs and illustrate how neuromorphic processors can successfully outperform traditional processors capabilities in a number of use cases. Nevertheless, the study is limited. These neuromorphic processors have a large architecture and are thus difficult to implement in an scalable form. Moreover, the present design of the current designs is still at its early development stage, hence making the use of its practical applications questionable. In addition, the research addresses the need for further optimizing interfacing these processors with current software systems to expand the utilities of these processors in the computing industry [157]-[164].

Liu et al. (2024) present the idea of 'SemiSynBio,' a new hybrid using synthetic biology with neuromorphic computing, in their article. It provides an innovative direction in the field through use of biological systems to improve the performance of artificial neuromorphic circuits. The novelty is in the use of biological material and mechanisms to make more adaptive, more efficient, and more scalable neuromorphic systems. These new possibilities for brain-like computing architectures that can self organize, self heal, closely mimicking natural neural networks are enabled through this approach. Furthermore, the paper introduces potentials of using them in bio-computing and next generation artificial intelligence systems. Criticism is noted, however, several limitations are noted. Much work remains to be done in the integration of biological components into computing systems where stability, reliability and scalability challenges remain unaddressed. We overcome this barrier by demonstrating that the complexity of providing consistent hybrid system performance in real world environments

translates to a small and stable system control structure. The paper acknowledges that ethical and safety issues relevant to bio-hybrid technologies require further research [165]-[171].

Table. 1: Key Innovations, Challenges, and Future Directions in Neuromorphic VLSI Circuit Design

Reference	Key Focus	Innovation/Concept	Application Area	Challenges Identified	Potential Solutions	Future Directions
Wang et al. (2024)	Photonic Neuromorphic Systems	Integration of photonics for improved speed and efficiency	High-speed data processing	Scalability of photonic systems	Hybrid photonic-electronic systems	Scaling photonics for broader applications
Kumar et al. (2023)	In-memory Architecture for ANN	Real-time scalable architecture for AI/ML	AI/ML applications	Memory bottleneck issues	Optimized memory architecture	Enhanced training efficiency in AI/ML hardware
Liu et al. (2022)	Bio-inspired 3D Neuromorphic Circuits	Enhanced computational efficiency in 3D circuits	3D neuromorphic architectures	Manufacturing complexity	3D printing technologies	Exploration of organic-based circuits
Li et al. (2024)	Memristive Neuromorphic Networks	Artificial neurons based on biological neural dynamics	Memristive systems	Stability and endurance	Robust memristor designs	Integration of bio-neural concepts
Nazari et al. (2022)	Spiking Neural Networks (SNNs)	Unsupervised learning for pattern recognition	Biologically inspired systems	Circuit complexity	Efficient spike coding methods	Improved hardware-software co-design for SNNs
Ahmed (2023)	Bio-Inspired Artificial Synapses	Soft biomaterial-based neuromorphic chips	Energy-efficient neuromorphic circuits	Material compatibility	Advanced bio-materials	Organic materials in neuromorphic synapses
Balaji et al. (2022)	Neuromorphic Architecture Design	New techniques for	Neuromorphic architecture design	Scalability challenges	Modular architecture approaches	Large-scale neuromorphic applications

		neuromorphic architecture				
Yang et al. (2020)	Biological Spike-Based Hardware	Efficient real-time spike-based systems	Spike-based hardware	Integration with conventional systems	Mixed-signal integration	Expansion of bio-inspired hardware systems
Mehonic et al. (2020)	Memristors in Neuromorphic Computing	In-memory computing and SNN acceleration	Memristive neuromorphic computing	Memristor reliability	Improved reliability testing	Broader deployment of memristor-based systems
Javanshir et al. (2022)	Algorithms & Neuromorphic Hardware	Hardware-algorithm co-design for SNNs	Spiking neural networks	Hardware-software integration	Co-design optimization tools	Refined algorithmic support for neuromorphic hardware
Rose et al. (2021)	Neuromorphic Processor Design	System-level design for neuromorphic computing	Computer processors	Area and power constraints	Low-power design techniques	Optimized processor designs for neuromorphic systems
Liu et al. (2024)	SemiSynBio for Neuromorphic Computing	Integration of synthetic biology in neuromorphic systems	Neuromorphic computing	Design complexity in synthetic biology	Collaboration with bio-engineering	Neuromorphic synthetic biology expansion

Recent advances in the field of neuromorphic VLSI circuit design are presented and a Table 1 shows the main innovations, challenges, and future directions of neuromorphic VLSI circuits. It shows promising work in the areas of memristive networks, spiking neural networks, and bio-inspired synaptic devices. Six identified challenges are scalability, energy efficiency, and the integration of artificial intelligence (AI) into neuromorphic architectures. On the other hand, future directions to enhance learning algorithms, improve in-memory computing, and optimize hardware software co-design for good performance. With this comprehensive overview, we provide a roadmap for overcoming current limitations and continuing to propel forward in neuromorphic computing technologies (Madrenas et al. (2009), Adomaitiene et al. (2021), Such et al. (2018)) [172]-[189].

1.1 Understanding Neuromorphic Computing

Neuromorphic computing is a fascinating field that draws inspiration from the human brain to create more efficient and powerful computing systems. We're diving into the world of brain-inspired AI, exploring how these innovative systems work and why they're so promising for the future of technology.

a. Biological Neural Networks

Let's start by looking at the biological neural networks that serve as the foundation for neuromorphic computing. Our brains are made up of billions of interconnected neurons, forming an intricate web of processing units. These neurons communicate through synapses, accepting input from other neurons or external stimuli. What's really interesting is how our brains learn and adapt. As we experience new things, the connections between neurons change. Some connections get stronger, new ones form, and unused ones may disappear. This flexibility allows us to process and store information in incredibly efficient ways. One of the coolest things about biological neural networks is their ability to handle complex tasks with relatively low power consumption. Our brains run on about 20 watts of power – that's less than a dim light bulb! This energy efficiency is something we're trying to replicate in neuromorphic chips [190]-[195].

Table. 2: Key Features of Neuromorphic Computing vs Traditional Computing

Feature	Neuromorphic Computing	Traditional Computing
Architecture	Mimics biological neural networks	Von Neumann architecture with separate memory and processing units
Computation Model	Event-driven, asynchronous, spiking neural networks	Clock-driven, synchronous, binary logic
Power Consumption	Ultra-low power, energy-efficient	Higher power consumption
Data Processing	Distributed and parallel processing	Sequential, centralized processing
Learning Mechanism	On-chip, real-time learning through synaptic weights adaptation	Software-based machine learning algorithms on traditional CPUs/GPUs
Scalability	High, suited for dense integration of neurons and synapses	Limited by heat and power constraints in large systems
Memory Usage	Integrated with processing (in-memory computation)	Separate memory and processing units
Applications	AI, robotics, real-time decision making, edge computing	General-purpose computing, traditional machine learning tasks

b. Artificial Neural Networks

Now, let's talk about artificial neural networks (ANNs), which are the stepping stones to neuromorphic computing. ANNs are mathematical models inspired by biological neurons, but they work a bit differently. In an ANN, we have layers of interconnected "neurons" that process information. Each connection has a weight, and these weights are adjusted during training to improve the network's performance. ANNs have shown impressive results in tasks like image recognition and natural language processing. However, traditional ANNs have some limitations. They often require powerful hardware and consume a lot of energy, especially when dealing with complex tasks. This is where neuromorphic computing comes in, aiming to bridge the gap between artificial and biological neural networks [196]-[199].

Table 3: Benefits of Intel Neuromorphic Chips for AI and VLSI Circuits

Aspect	Intel Neuromorphic Chips	Bio-Inspired VLSI Circuits
Energy Efficiency	Low-power consumption for energy-constrained AI	Mimics brain's efficiency in information processing
Real-Time Processing	Real-time learning and inference for dynamic tasks	High-speed event-driven processing
Scalability	Highly scalable with dense neuron-synapse integration	Scalable architecture for complex computations
Adaptability	On-chip learning for changing environments	Flexible and adaptive to changes in input patterns
Latency	Low latency due to event-driven architecture	Minimal delay in response due to parallelism in processing
Hardware Efficiency	Optimized for AI applications with custom hardware	Compact and efficient circuits inspired by neural architecture
Target Applications	Robotics, AI edge devices, autonomous systems	AI, neuroprosthetics, brain-machine interfaces

1.2 Spiking Neural Networks

Spiking Neural Networks (SNNs) are the next step in our journey towards brain-like computing. These networks take inspiration from biological neurons in a more direct way, incorporating the concept of time and using spikes to transmit information. In an SNN, neurons only fire when they receive enough input to reach a certain threshold. This event-driven approach is more energy-efficient than traditional ANNs, as computation only happens when necessary. It's like our brains – we don't constantly process every bit of information around us, but we react when something important happens. SNNs are particularly exciting for neuromorphic chips because they can be implemented using analog circuits that mimic the behavior of biological neurons. This allows for incredibly efficient processing, bringing us closer to the energy efficiency of the human brain. As we continue to develop neuromorphic

technology, we're seeing some amazing advancements. Intel's neuromorphic chip, for example, is pushing the boundaries of what's possible in this field. These chips are designed to process information in ways that are more similar to our brains, opening up new possibilities for AI and machine learning applications. The future of neuromorphic computing is bright, with potential applications ranging from more efficient edge computing devices to advanced robotics and even brain-computer interfaces. As we continue to unlock the secrets of how our brains process information, we're getting closer to creating AI systems that can think and learn more like we do [200]-[206].

2. Intel's Loihi: Architecture and Capabilities

We're diving into Intel's groundbreaking neuromorphic chip, Loihi, which is pushing the boundaries of brain-inspired AI. This innovative technology is designed to process information in ways that are more similar to our brains, opening up new possibilities for AI and machine learning applications.

Table. 4: Key Architectural Features of Intel's Loihi Neuromorphic Chip

Feature	Description
Core Count	128 neuromorphic cores, each simulating a large number of spiking neurons
Neuron Simulation Capacity	Capable of simulating over 130,000 neurons and 130 million synapses
Spiking Neural Networks (SNNs)	Uses SNNs that mimic the spike-based communication of biological neurons
Asynchronous Processing	Event-driven, asynchronous processing for energy-efficient computations
Plasticity Engine	Supports real-time learning with programmable synaptic learning rules
In-Memory Computation	Combines memory and processing within each core to reduce data transfer overhead
Scalability	Designed to be scalable, enabling large networks of neurons across multiple chips
Power Efficiency	Optimized for ultra-low-power operation compared to traditional AI chips

2.1 Core Design

At the heart of Loihi's architecture is a manycore mesh comprising 128 neuromorphic cores, three embedded x86 processor cores, and off-chip communication interfaces. This design allows for efficient, parallel processing of neural network computations. Each neuromorphic core implements 1,024 primitive spiking neural units, called compartments, which are grouped into sets of trees constituting neurons. What sets Loihi apart is its asynchronous design. The chip uses an asynchronous

network-on-chip (NoC) to transport all communication between cores in the form of packetized messages. This approach minimizes active power by exploiting the sparsity of neural spike events in time and across the array. As a result, Loihi can achieve per-core neuron update rates exceeding 10MHz in a 1V process corner [207]-[211].

2.2 Neural Network Implementation

Loihi implements a spiking neural network (SNN) that closely mimics the behavior of biological neural networks. Instead of manipulating signals, the chip sends spikes along activated synapses. This event-driven approach is more energy-efficient than traditional artificial neural networks, as computation only happens when necessary. The chip supports a range of features that make it highly flexible and powerful. It can model up to 130,000 synthetic compartmental neurons and 130 million synapses. Loihi also includes several computational primitives related to other active areas of SNN algorithmic research, such as dendritic compartments, synaptic delays, and stochastic synaptic noise. One of Loihi's standout features is its support for hierarchical connectivity patterns. This allows for the mapping of deep convolutional networks optimized for vision and audio sensing tasks. The chip's neural model is based on standard leaky integrate-and-fire dynamics, extended with features like reward-modulated spike-timing-dependent plasticity and axonal and refractory delays [212]-[218].

Table. 5: Capabilities of Intel's Loihi for AI/ML Applications

Capability	Description
Real-Time Learning	On-chip learning enables real-time adaptation to changing environments
Edge Computing	Ultra-low power consumption makes it suitable for edge AI/ML applications
Pattern Recognition	Efficiently handles pattern recognition tasks such as image and speech processing
Autonomous Systems	Supports AI applications in autonomous systems, including robotics and vehicles
Energy Efficiency for AI/ML	Provides significant reductions in energy consumption for AI/ML tasks
Latency Reduction	Low-latency processing due to the event-driven architecture
Parallel Processing	Processes information in a massively parallel manner, similar to biological brains
AI Security	Potential for neuromorphic chips to improve hardware security and detection of anomalies

2.3 Learning and Adaptation

Perhaps the most exciting aspect of Loihi is its ability to learn and adapt. Each core includes a programmable learning engine that can evolve synaptic state variables over time as a function of historical spike activity. This on-chip learning capability is a game-changer for neuromorphic computing. Loihi's learning engine supports a wide range of learning rules, from simple pairwise spike-

timing-dependent plasticity (STDP) to more complex rules that reference both rate-averaged and spike-timing traces. These rules are microcode programmable, giving researchers and developers unprecedented flexibility in designing learning algorithms. The chip's learning capabilities have shown promising results in various applications. For instance, Intel and its collaborators have demonstrated continual interactive learning on Loihi, measuring up to 175x lower energy consumption to learn a new object instance compared to conventional methods running on a CPU. This has significant implications for future robotic assistants that need to interact with unconstrained environments [219]-[224].

Loihi's unique approach to learning satisfies the locality constraint, which is crucial for scaling up adaptive networks efficiently. This means that learning in Loihi proceeds in an online manner, where training samples are sent to the network sequentially, and the network adapts in real-time. As we continue to explore the potential of neuromorphic computing, Loihi stands out as a powerful tool for researchers and developers. Its innovative architecture and learning capabilities are paving the way for more efficient, adaptive, and brain-like AI systems. The future of AI hardware is looking increasingly neuromorphic, and Intel's Loihi is at the forefront of this exciting revolution [225]-[229].

3. Bio-Inspired VLSI Circuit Innovations

We're witnessing a fascinating convergence of biology and technology in the realm of neuromorphic computing. By drawing inspiration from the intricate workings of the human brain, we're developing innovative VLSI (Very Large Scale Integration) circuits that are pushing the boundaries of AI hardware. These bio-inspired designs are paving the way for more efficient and powerful neuromorphic chips, like Intel's groundbreaking Loihi [230]-[232].

Table. 6: Bio-Inspired VLSI Circuit Innovations and Advantages for AI/ML Applications

Aspect	Description
Neuromorphic Architectures	Mimics biological neural networks for efficient parallel data processing
Spiking Neural Networks (SNNs)	Uses event-driven, spike-based communication to enhance energy efficiency
In-Memory Computing	Combines memory and processing units to reduce data transfer delays and power consumption
Synaptic Plasticity Circuits	Implements real-time learning through synaptic weight adaptation
Low-Power Design	Reduces power consumption, making it suitable for energy-constrained environments
3D VLSI Integration	Increases neuron and synapse density, enabling greater performance and scalability
Energy Efficiency	Consumes less power compared to traditional AI hardware, ideal for edge AI/ML tasks

Real-Time Processing	Supports on-the-fly learning and real-time decision making in dynamic environments
Scalability	Allows scaling for large neural networks and complex AI models
Low Latency	Event-driven architectures reduce processing delays, improving performance in time-sensitive tasks

3.1 Analog Computation

One of the most exciting aspects of bio-inspired VLSI circuits is their use of analog computation. Unlike traditional digital systems, analog circuits can process information in a way that's much closer to how our brains work. We're seeing a shift towards mixed-signal designs that combine the best of both worlds – the precision of digital circuits and the efficiency of analog processing. In our research, we've found that analog circuits are particularly well-suited for implementing neural network primitives. These circuits can directly exploit the physics of the devices to carry out complex computations, such as exponential and logarithmic functions. By operating transistors in the subthreshold region, we can achieve ultra-low power consumption while still maintaining the ability to perform sophisticated calculations [233]-[239].

3.2 Mixed-Signal Designs

The future of neuromorphic architecture lies in mixed-signal designs that seamlessly integrate analog and digital components. We're developing compact and energy-efficient subthreshold analog synapse and neuron circuits that can be implemented in advanced scaled processes, like 28nm FD-SOI (Fully-Depleted Silicon on Insulator). These mixed-signal designs allow us to maximize density with analog/digital synaptic weight configurations. We're also implementing techniques to minimize the effect of channel leakage current, enabling efficient analog computation based on picoampere to nanoampere currents. This approach is crucial for creating large-scale, multi-neuron, multi-core neuromorphic computing architectures that can rival the efficiency of the human brain [240]-[242].

3.3 Novel Materials and Devices

To truly replicate the capabilities of biological neural networks, we need to explore novel materials and devices. Our research has led us to investigate a wide range of innovative components that can serve as artificial counterparts to biological actors in the brain's structure and operation. One exciting development is the use of memristors in building artificial cochleas. These devices, with their ability to "remember" past states, are proving to be excellent candidates for configurable, highly parallel, and highly efficient auditory systems for neuromorphic robots. We've also been exploring the potential of superconducting Quantum Phase Slip Junctions (QPSJs) in neuromorphic circuits, which could lead to high-speed and low-power spiking neural networks capable of both supervised and unsupervised learning. Another promising area is the development of Insulator-Metal Transition (IMT) device-based oscillators. Our studies have shown that NbO₂-based IMT oscillators with non-volatile Li-based electrochemical random access memory (Li-ECRAM) have the potential for high network performance, thanks to their linear conductance modulation characteristics. As we continue to push the boundaries of neuromorphic technology, these bio-inspired VLSI circuit innovations are bringing

us closer to creating AI systems that can truly think and learn like the human brain. The future of neuromorphic computing is bright, and we're excited to see how these advancements will shape the next generation of AI hardware [243]-[249].

4. Applications Driving Neuromorphic Computing

We're witnessing a revolution in computing, and neuromorphic technology is at the forefront. Intel's neuromorphic chip and other brain-inspired AI systems are opening up exciting possibilities across various fields. Let's explore some of the key applications that are driving the development of neuromorphic computing.

Table. 7: Applications Driving Neuromorphic Computing

Application Area	Description
Autonomous Systems	Neuromorphic chips enable real-time decision-making and low-power processing in autonomous vehicles, drones, and robots.
Edge Computing	Ultra-low power consumption makes neuromorphic chips ideal for AI/ML tasks at the edge, such as IoT devices and smart sensors.
Robotics	Mimics human-like perception, learning, and adaptation in robots, improving their ability to interact with and respond to changing environments.
AI for Healthcare	Real-time data processing for medical devices, neuroprosthetics, and brain-machine interfaces, allowing for personalized healthcare solutions.
Speech and Image Recognition	Neuromorphic circuits enhance pattern recognition capabilities, reducing power consumption for tasks like voice assistants and visual recognition.
Cybersecurity	Neuromorphic hardware can be used for anomaly detection and improving security through real-time threat detection with minimal latency.
Neuroprosthetics	Bio-inspired designs support the development of brain-machine interfaces, enabling more natural control over prosthetic limbs and neural therapies.
Smart Cities	Low-power AI for managing smart infrastructure, including energy management, traffic monitoring, and environmental sensing.

4.1 Computer Vision

Computer vision is one area where neuromorphic chips are making significant strides. These brain-inspired AI systems are particularly well-suited for processing complex visual inputs quickly and efficiently. We're seeing remarkable advancements in areas like autonomous vehicles, where

neuromorphic systems can process sensory data in real-time, enabling swift navigation decisions. Smart cameras enhanced with neuromorphic computing are another exciting application. These devices can perform on-the-fly image processing for tasks like surveillance, traffic management, and crowd monitoring. What's really impressive is how the efficiency of neuromorphic chips allows these smart cameras to operate at lower power, extending their operational lifespan when deployed in the field. One standout example is the Tianjic chip, developed by Chinese scientists. This neuromorphic chip has been used to power a self-driving bike capable of following a person, navigating obstacles, and responding to voice commands. With 40,000 neurons and 10 million synapses, it performs 160 times better and 120,000 times more efficiently than a comparable GPU. This showcases the potential of neuromorphic architecture in creating more intelligent and responsive visual systems [250]-[258].

4.2 Natural Language Processing

Natural Language Processing (NLP) is another field that's benefiting from the power of neuromorphic computing. As we deal with ever-increasing amounts of text data from the web, there's a growing need for efficient ways to process and understand this information. Neuromorphic chips are stepping up to this challenge, offering new possibilities for high-quality analysis of user input on mobile devices with minimal battery drain. We're seeing exciting developments in tasks like sentiment analysis and question classification. For instance, researchers have developed a system called 'TrueHappiness' that uses a neural network to predict the 'happiness' associated with given words. This system, designed for the TrueNorth neuromorphic chip, demonstrates how we can map traditional deep learning systems to neuromorphic platforms. The efficiency of neuromorphic computing in NLP tasks could lead to data centers that understand queries while consuming far less power than conventional high-performance computers. This has huge implications for making AI more accessible and sustainable [259]-[271].

4.3 Robotics and Control Systems

Neuromorphic computing is also making waves in robotics and control systems. These brain-inspired AI systems enhance sensory processing and movement control, enabling robots to interpret and interact with their environment more effectively. This is crucial for tasks requiring autonomous decision-making. We're seeing neuromorphic chips being used to implement navigation systems for roaming, obstacle-avoidance robots. For example, researchers have created a spiking neural network autonomous robot control system using an array of neuromorphic computing elements built on an FPGA. This system allows a mobile robot to navigate a dynamically changing environment, showcasing the potential of neuromorphic architecture in creating more adaptive and responsive robotic systems [272]-[279].

The applications of neuromorphic computing in robotics extend beyond navigation. These systems are being used to develop more sophisticated capabilities like object identification and tracking. As neuromorphic technology continues to advance, we can expect to see robots that are more capable, efficient, and able to operate in complex, unpredictable environments. As we continue to explore the potential of neuromorphic computing, we're uncovering new possibilities for creating more intelligent, efficient, and responsive systems across a wide range of applications. From enhancing our visual processing capabilities to revolutionizing how we interact with language and control robotic systems,

neuromorphic chips are paving the way for a new era of AI that's more brain-like in its approach to problem-solving [280]-[297].

5. The Future of AI Hardware

As we look ahead, the landscape of AI hardware is set to undergo a dramatic transformation. We're witnessing a convergence of cutting-edge technologies that promise to revolutionize how we approach artificial intelligence. The future of AI hardware is not just about incremental improvements; it's about reimagining the very foundations of computing.

Table. 8: The Future of AI Hardware

Key Focus Area	Description
Energy Efficiency	Future AI hardware will prioritize low-power designs, enabling AI/ML applications in energy-constrained environments such as edge computing and mobile devices.
Neuromorphic Computing	Bio-inspired architectures like neuromorphic chips will lead the way in mimicking brain-like efficiency, with event-driven processing and real-time learning capabilities.
In-Memory Computing	AI hardware will integrate memory and processing to reduce the bottlenecks caused by data transfer, improving speed and energy efficiency.
3D Integration	3D IC stacking will increase the density of processing units and improve performance by allowing larger neural networks on smaller chips.
Scalability	Next-generation AI hardware will focus on scalability to accommodate the increasing complexity and size of AI models, particularly for deep learning applications.
Real-Time Processing	Hardware will support faster decision-making in real-time applications like robotics, autonomous systems, and smart sensors, enabling instant responses to environmental changes.
Customizable AI Chips	AI-specific chips with customizable architectures will allow more specialized and optimized performance for tasks such as natural language processing and computer vision.
Security and Trust	AI hardware will incorporate security features to prevent malicious attacks, ensuring trustworthy AI in sensitive applications like finance and healthcare.

5.1 Hybrid Computing Systems

We're seeing a shift towards hybrid computing systems that combine the best of different AI approaches. These systems are designed to leverage the strengths of various techniques, resulting in

more powerful and efficient AI solutions. By integrating machine learning with symbolic AI, we're creating systems that can process information in ways that are closer to human cognition. One of the most exciting aspects of hybrid AI is its ability to handle complex cognitive problems more effectively. We're developing systems that can perform tasks requiring both pattern recognition and logical reasoning. This approach is particularly promising for natural language processing, where understanding context and meaning is crucial. The scalability of hybrid systems is another key advantage. As we continue to push the boundaries of AI, these systems can adapt and grow to meet increasing demands. This scalability is essential for businesses looking to implement AI solutions that can evolve with their needs [298]-[302].

5.2 Neuromorphic-Quantum Integration

The integration of neuromorphic computing with quantum AI represents a paradigm shift in how we approach complex computational problems. We're exploring ways to combine the brain-inspired architecture of neuromorphic chips with the immense processing power of quantum computing [303]-[304].

This integration offers several exciting possibilities:

1. **Improved Energy Efficiency:** Neuromorphic systems are designed to operate with minimal energy consumption, making them ideal for quantum applications that require significant computational resources.
2. **Real-time Processing:** The event-driven nature of neuromorphic computing allows for real-time data processing, crucial for quantum AI applications that demand immediate responses to dynamic inputs.
3. **Enhanced Parallel Processing:** Neuromorphic systems excel at parallel processing, enabling them to handle multiple data streams simultaneously. This is particularly advantageous in quantum AI, where processing vast amounts of data in real-time is essential.

5.3 Scaling to Brain-Level Complexity

As we continue to develop neuromorphic chips and quantum computing technologies, we're inching closer to creating systems that can rival the complexity of the human brain. While we're still far from fully replicating the brain's capabilities, we're making significant strides in that direction. Current neuromorphic chips, like Intel's Loihi, are already capable of simulating millions of neurons. As we scale up these systems, we're exploring the potential for chips with billions of neurons, bringing us closer to brain-level complexity. This scaling presents both challenges and opportunities [305]-[316]:

1. **Increased Processing Power:** Larger neuromorphic systems will be capable of handling more complex AI tasks, potentially revolutionizing fields like autonomous driving and advanced robotics.
2. **Novel Materials and Devices:** To achieve this level of scaling, we're investigating new materials and devices that can enhance the performance of neuromorphic and quantum systems.
3. **Energy Efficiency at Scale:** As we increase the size and complexity of these systems, maintaining energy efficiency becomes crucial. We're developing innovative approaches to minimize power consumption while maximizing computational capabilities.

The future of AI hardware is bright, with neuromorphic chips and quantum computing leading the charge. As we continue to push the boundaries of what's possible, we're creating systems that are not just more powerful, but also more efficient and adaptable. The integration of these technologies promises to unlock new possibilities in AI, bringing us closer to creating truly intelligent machines.

6. Conclusion

The journey through the world of neuromorphic computing and bio-inspired VLSI circuits has shown us the incredible potential of brain-like AI systems. Intel's Loihi chip stands out as a game-changer, showcasing how mimicking the human brain can lead to more efficient and adaptable AI hardware. This approach has a big impact on various fields, from computer vision to robotics, paving the way for smarter, more responsive technologies that can handle complex tasks with less energy. Looking ahead, the future of AI hardware seems bright and full of possibilities. The combination of neuromorphic computing with quantum AI and the development of hybrid systems promise to take us closer to brain-level complexity. As we keep pushing the boundaries, we're not just making AI more powerful, but also more efficient and in tune with how our brains work. This progress opens up new doors to tackle complex problems and create AI systems that can truly think and learn like we do.

References

- [1] Wang, Wenju, Haoran Zhou, Wei Li, and Elena Goi. "Neuromorphic computing." In *Neuromorphic Photonic Devices and Applications*, pp. 27-45. Elsevier, 2024.
- [2] Adomaitienė, Elena, Steponas Ašmontas, Skaidra Bumelienė, and Arūnas Tamaševičius. "Controllability of the unijunction transistor based integrate-and-fire electronic spiking neuron." *AEU-International Journal of Electronics and Communications* 133 (2021): 153666.
- [3] Kumar, Abhash, Sai Manohar Beeraka, Jawar Singh, and Bharat Gupta. "An On-Chip Trainable and Scalable In-Memory ANN Architecture for AI/ML Applications." *Circuits, Systems, and Signal Processing* 42, no. 5 (2023): 2828-2851.
- [4] Liu, Xuhai, Fengyun Wang, Jie Su, Ye Zhou, and Seeram Ramakrishna. "Bio-Inspired 3D Artificial Neuromorphic Circuits." *Advanced Functional Materials* 32, no. 22 (2022): 2113050.
- [5] Tozlu, Ömer Faruk, Fırat Kaçar, and Yunus Babacan. "Electronically controllable neuristor based logic gates and their applications." *AEU-International Journal of Electronics and Communications* 138 (2021): 153834.
- [6] Zhang, Q., H. Deng, and K. Song. "Latest VLSI Techniques for 3nm Technology for Building Efficient AI Chips." *Fusion of Multidisciplinary Research, An International Journal* 5, no. 2 (2024): 654-670.
- [7] Li, Xiaosong, Jingru Sun, Yichuang Sun, Chunhua Wang, Qinghui Hong, Sichun Du, and Jiliang Zhang. "Design of artificial neurons of memristive neuromorphic networks based on biological neural dynamics and structures." *IEEE Transactions on Circuits and Systems I: Regular Papers* (2024).
- [8] Madrenas, Jordi, Daniel Fernández, Jordi Cosp, Luis Martínez-Alvarado, Eduard Alarcón, Eva Vidal, and Gerard Villar. "Self-controlled 4-transistor low-power min-max current selector." *AEU-International Journal of Electronics and Communications* 63, no. 10 (2009): 871-876.

- [9] Nazari, Soheila, Alireza Keyanfar, and Marc M. Van Hulle. "Neuromorphic circuit based on the un-supervised learning of biologically inspired spiking neural network for pattern recognition." *Engineering Applications of Artificial Intelligence* 116 (2022): 105430.
- [10] Ahmed, Tanvir. "Bio-inspired artificial synapses: Neuromorphic computing chip engineering with soft biomaterials." *Memories-Materials, Devices, Circuits and Systems* 6 (2023): 100088.
- [11] Šuch, O., M. Klimo, N. T. Kemp, and O. Škvarek. "Passive memristor synaptic circuits with multiple timing dependent plasticity mechanisms." *AEU-International Journal of Electronics and Communications* 96 (2018): 252-259.
- [12] Ava, Oliver, Muhammad Oscar, and Tommy George. "The Impact and Prevention of Latch-up in CMOS in VLSI Design." *Fusion of Multidisciplinary Research, An International Journal* 1.01 (2020): 1-13.
- [13] Balaji, V. Nithin, P. Bala Srinivas, and Mahesh K. Singh. "Neuromorphic advancements architecture design and its implementations technique." *Materials Today: Proceedings* 51 (2022): 850-853.
- [14] Yang, Jia-Qin, Ruopeng Wang, Yi Ren, Jing-Yu Mao, Zhan-Peng Wang, Ye Zhou, and Su-Ting Han. "Neuromorphic engineering: from biological to spike-based hardware nervous systems." *Advanced Materials* 32, no. 52 (2020): 2003610.
- [15] Mahmoodi, Alireza G., and Adib Abrishamifar. "A class AB ultra-low-power asymmetrical structured current multiplier." *AEU-International Journal of Electronics and Communications* 186 (2024): 155470.
- [16] Mehonic, Adnan, Abu Sebastian, Bipin Rajendran, Osvaldo Simeone, Eleni Vasilaki, and Anthony J. Kenyon. "Memristors—From in-memory computing, deep learning acceleration, and spiking neural networks to the future of neuromorphic and bio-inspired computing." *Advanced Intelligent Systems* 2, no. 11 (2020): 2000085.
- [17] Javanshir, Amirhossein, Thanh Thi Nguyen, MA Parvez Mahmud, and Abbas Z. Kouzani. "Advancements in algorithms and neuromorphic hardware for spiking neural networks." *Neural Computation* 34, no. 6 (2022): 1289-1328.
- [18] Rose, Garrett S., Mst Shamim Ara Shawkat, Adam Z. Foshie, John J. Murray, and Md Musabbir Adnan. "A system design perspective on neuromorphic computer processors." *Neuromorphic Computing and Engineering* 1, no. 2 (2021): 022001.
- [19] Hernández, Fernanda, Leonardo Sánchez, Gabriela González, and Andrés Ramírez. "Revolutionizing CMOS VLSI with Innovative Memory Design Techniques." *Fusion of Multidisciplinary Research, An International Journal* 3, no. 2 (2022): 366-379.
- [20] Liu, Ruicun, Tuoyu Liu, Wuge Liu, Boyu Luo, Yuchen Li, Xinyue Fan, Xianchao Zhang, Wei Cui, and Yue Teng. "SemiSynBio: A new era for neuromorphic computing." *Synthetic and Systems Biotechnology* (2024).
- [21] Yesil, Abdullah, and Yunus Babacan. "Tunable memristor employing only four transistors." *AEU-International Journal of Electronics and Communications* 169 (2023): 154763.
- [22] Suba, R., & Satheeskumar, R. (2016). Efficient cluster-based congestion control in wireless mesh network. *International Journal of Communication and Computer Technologies*, 4(2), 96-101.

- [23] Rimada, Y., Mrinh, K.L., & Chuonghan. (2024). Unveiling the printed monopole antenna: Versatile solutions for modern wireless communication. *National Journal of Antennas and Propagation*, 6(1), 1–5.
- [24] Udhayakumar, A., Ramya, K. C., Vijayakumar, P., Sheeba Rani, S., Balamanikandan, A., & Saranya, K. (2024). Reversible Vedic Direct Flag Divider in Key Generation of RSA Cryptography. *Journal of VLSI Circuits and Systems*, 6(2), 75–83. <https://doi.org/10.31838/jvcs/06.02.08>
- [25] Tang, U., Krezger, H., & LonnerbyRakob. (2024). Design and validation of 6G antenna for mobile communication. *National Journal of Antennas and Propagation*, 6(1), 6–12.
- [26] Muralidharan, J. (2024). Advancements in 5G technology: Challenges and opportunities in communication networks. *Progress in Electronics and Communication Engineering*, 1(1), 1–6. <https://doi.org/10.31838/PECE/01.01.01>
- [27] Alnumay, W.S. (2024). The past and future trends in IoT research. *National Journal of Antennas and Propagation*, 6(1), 13–22.
- [28] Bhowmik, S., Majumder, T., & Bhattacharjee, A. (2024). A Low Power Adiabatic Approach for Scaled VLSI Circuits. *Journal of VLSI Circuits and Systems*, 6(1), 1–6. <https://doi.org/10.31838/jvcs/06.01.01>
- [29] Klavin, C. (2024). Analysing antennas with artificial electromagnetic structures for advanced performance in communication system architectures. *National Journal of Antennas and Propagation*, 6(1), 23–30.
- [30] Yang, C. S., Lu, H., & Qian, S. F. (2024). Fine tuning SSP algorithms for MIMO antenna systems for higher throughputs and lesser interferences. *International Journal of Communication and Computer Technologies*, 12(2), 1-10. <https://doi.org/10.31838/IJCCTS/12.02.01>
- [31] Soh, H., & Keljovic, N. (2024). Development of highly reconfigurable antennas for control of operating frequency, polarization, and radiation characteristics for 5G and 6G systems. *National Journal of Antennas and Propagation*, 6(1), 31–39.
- [32] Botla, A., Kanaka Durga, G., & Paidimarry, C. (2024). Development of Low Power GNSS Correlator in Zynq SoC for GPS and GLONSS. *Journal of VLSI Circuits and Systems*, 6(2), 14–22. <https://doi.org/10.31838/jvcs/06.02.02>
- [33] Raktur, H., & Jea, T. (2024). Design of compact wideband wearable antenna for health care and internet of things system. *National Journal of Antennas and Propagation*, 6(1), 40–48.
- [34] Sulyukova, L. (2025). Latest innovations in composite material technology. *Innovative Reviews in Engineering and Science*, 2(2), 1-8. <https://doi.org/10.31838/INES/02.02.01>
- [35] Halily, R., & Shen, M. (2024). Directing techniques for high frequency antennas for use in next-generation telecommunication countries. *National Journal of Antennas and Propagation*, 6(1), 49–57.
- [36] Anandhi, S., Rajendrakumar, R., Padmapriya, T., Manikanthan, S. V., Jebanazer, J. J., & Rajasekhar, J. (2024). Implementation of VLSI Systems Incorporating Advanced Cryptography Model for FPGA-IoT Application. *Journal of VLSI Circuits and Systems*, 6(2), 107–114. <https://doi.org/10.31838/jvcs/06.02.12>

- [37] Shum, A. (2024). System-level architectures and optimization of low-cost, high-dimensional MIMO antennas for 5G technologies. *National Journal of Antennas and Propagation*, 6(1), 58–67.
- [38] Antoniewicz, B., & Dreyfus, S. (2024). Techniques on controlling bandwidth and energy consumption for 5G and 6G wireless communication systems. *International Journal of Communication and Computer Technologies*, 12(2), 11-20. <https://doi.org/10.31838/IJCCTS/12.02.02>
- [39] Yeonjin, K., Hee-Seob, K., Hyunjae, L., & Sungho, J. (2023). Venting the potential of wirelessly reconfigurable antennas: Innovations and future directions. *National Journal of Antennas and Propagation*, 5(2), 1–6.
- [40] Vijay, V., Pittala, C. S., Usha Rani, A., Shaik, S., Saranya, M. V., Vinod Kumar, B., Praveen Kumar, R. E. S., & Vallabhuni, R. R. (2022). Implementation of Fundamental Modules Using Quantum Dot Cellular Automata. *Journal of VLSI Circuits and Systems*, 4(1), 12–19. <https://doi.org/10.31838/jvcs/04.01.03>
- [41] Kigarura, M., Okunki, L., & Nbende, P. (2023). Primary frontiers in designing and benchmarking the applications of helical antennas. *National Journal of Antennas and Propagation*, 5(2), 7–13.
- [42] Muralidharan, J. (2024). Optimization techniques for energy-efficient RF power amplifiers in wireless communication systems. *SCCTS Journal of Embedded Systems Design and Applications*, 1(1), 1-6. <https://doi.org/10.31838/ESA/01.01.01>
- [43] Kurshid, B., Rshour, L., Ali, M. W., Al-Fares, R., & Fahad, A. J. (2023). The potential of ultra-wideband printed rectangular-based monopole antennas. *National Journal of Antennas and Propagation*, 5(2), 14–20.
- [44] Vijay, V., Sreevani, M., Mani Rekha, E., Moses, K., Pittala, C. S., Sadulla Shaik, K. A., Koteshwaramma, C., Jashwanth Sai, R., & Vallabhuni, R. R. (2022). A Review on N-Bit Ripple-Carry Adder, Carry-Select Adder, and Carry-Skip Adder. *Journal of VLSI Circuits and Systems*, 4(1), 27–32. <https://doi.org/10.31838/jvcs/04.01.05>
- [45] Lemeon, M., Regash, J., & Leyene, T. (2023). The role and evaluation of inductive coupling in antenna design. *National Journal of Antennas and Propagation*, 5(2), 21–28.
- [46] Dorofte, M., & Krein, K. (2024). Novel approaches in AI processing systems for their better reliability and function. *International Journal of Communication and Computer Technologies*, 12(2), 21-30. <https://doi.org/10.31838/IJCCTS/12.02.03>
- [47] Beken, K., Caddwine, H., Kech, R., & Mlein, M. (2023). Electromagnetic sounding in antennas using near-field measurement techniques. *National Journal of Antennas and Propagation*, 5(2), 29–35.
- [48] Abdul, A. M., & Nelakuditi, U. R. (2021). A New Blind Zone Free PFD in Fractional-N PLL for Bluetooth Applications. *Journal of VLSI Circuits and Systems*, 3(1), 19–24. <https://doi.org/10.31838/jvcs/03.01.04>
- [49] Miladh, A., Leila, I., & Nabeel, A. Y. (2023). Integrating connectivity into fabric: Wearable textile antennas and their transformative potential. *National Journal of Antennas and Propagation*, 5(2), 36–42.

- [50] Borhan, M. N. (2025). Exploring smart technologies towards applications across industries. *Innovative Reviews in Engineering and Science*, 2(2), 9-16. <https://doi.org/10.31838/INES/02.02.02>
- [51] Wei, L., & Lau, W. C. (2023). Modelling the power of RFID antennas by enabling connectivity beyond limits. *National Journal of Antennas and Propagation*, 5(2), 43–48.
- [52] Abdul, A. M., & Nelakuditi, U. R. (2021). A New Blind Zone Free PFD in Fractional-N PLL for Bluetooth Applications. *Journal of VLSI Circuits and Systems*, 3(1), 19–24. <https://doi.org/10.31838/jvcs/03.01.04>
- [53] Roper, S., & Bar, P. (2024). Secure computing protocols without revealing the inputs to each of the various participants. *International Journal of Communication and Computer Technologies*, 12(2), 31-39. <https://doi.org/10.31838/IJCCTS/12.02.04>
- [54] Maidanov, K., & Fratlin, H. (2023). Antennas and propagation of waves connecting the world wirelessly. *National Journal of Antennas and Propagation*, 5(1), 1–5.
- [55] Yaremko, H., Stoliarchuk, L., Huk, L., Zapotichna, M., & Drapaliuk, H. (2024). Transforming Economic Development through VLSI Technology in the Era of Digitalization. *Journal of VLSI Circuits and Systems*, 6(2), 65–74. <https://doi.org/10.31838/jvcs/06.02.07>
- [56] Frire, G. F., de Mindonça, F., Smith, O. L. M., & Kantor, K. N. (2023). Typical constructs in unveiling the horizontal wire antenna. *National Journal of Antennas and Propagation*, 5(1), 6–12.
- [57] Uvarajan, K. P. (2024). Integration of artificial intelligence in electronics: Enhancing smart devices and systems. *Progress in Electronics and Communication Engineering*, 1(1), 7–12. <https://doi.org/10.31838/PECE/01.01.02>
- [58] Mleh, K. L., Klabi, H., & Sikalu, K. P. (2023). Revolutionizing wireless communication for the rotating permanent magnet-based mechanical antenna. *National Journal of Antennas and Propagation*, 5(1), 13–17.
- [59] Smith, O. J. M., de Mendonça, F., Kantor, K. N., Zaky, A. A., & Freire, G. F. (2022). Ultra Low Potential Operated Fundamental Arithmetic Module Design for High-Throughput Applications. *Journal of VLSI Circuits and Systems*, 4(1), 52–59. <https://doi.org/10.31838/jvcs/04.01.08>
- [60] Luedke, R. H., Kingdone, G. C., Li, Q. H., & Noria, F. (2023). Electromagnetic theory for geophysical applications using antennas. *National Journal of Antennas and Propagation*, 5(1), 18–25.
- [61] El-Saadawi, E., Abohamama, A. S., & Alrahmawy, M. F. (2024). IoT-based optimal energy management in smart homes using harmony search optimization technique. *International Journal of Communication and Computer Technologies*, 12(1), 1-20. <https://doi.org/10.31838/IJCCTS/12.01.01>
- [62] Monson, A. K., & Matharine, L. (2023). Unlocking wireless potential: The four-element MIMO antenna. *National Journal of Antennas and Propagation*, 5(1), 26–32.
- [63] Beyene, F., Negash, K., Semeon, G., & Getachew, B. (2023). CMOS Technology: Conventional Module Design for Faster Data Computations. *Journal of VLSI Circuits and Systems*, 5(1), 42–48. <https://doi.org/10.31838/jvcs/05.01.06>

- [64] Jakhir, C., Rudevtagva, R., & Riunaa, L. (2023). Advancements in the novel reconfigurable Yagi antenna. *National Journal of Antennas and Propagation*, 5(1), 33–38.
- [65] Hoa, N. T., & Voznak, M. (2025). Critical review on understanding cyber security threats. *Innovative Reviews in Engineering and Science*, 2(2), 17-24. <https://doi.org/10.31838/INES/02.02.03>
- [66] Zakir, F., & Rozman, Z. (2023). Pioneering connectivity using the single-pole double-throw antenna. *National Journal of Antennas and Propagation*, 5(1), 39–44.
- [67] Hugh, Q., Soria, F., Kingdon, C. C., & Luedke, R. G. (2022). Fundamental Data Separator Using Threshold Logic at Low-Supply Voltages. *Journal of VLSI Circuits and Systems*, 4(2), 30–37. <https://doi.org/10.31838/jvcs/04.02.05>
- [68] Metachew, K., Nemeon, L., Egash, D., & Teyene, K. (2022). Breaking boundaries: The triple-band MIMO antenna. *National Journal of Antennas and Propagation*, 4(2), 1–6.
- [69] Uvarajan, K. P., & Usha, K. (2024). Implement a system for crop selection and yield prediction using random forest algorithm. *International Journal of Communication and Computer Technologies*, 12(1), 21-26. <https://doi.org/10.31838/IJCCTS/12.01.02>
- [70] Moh, K. T., Jiang, V., Leo, K. W., & Diu, M. L. (2022). Unlocking the potential of mechanical antennas for revolutionizing wireless communication. *National Journal of Antennas and Propagation*, 4(2), 7–12.
- [71] Saritha, M., Chaitanya, K., Vijay, V., Aishwarya, A., Yadav, H., & Durga Prasad, G. (2022). Adaptive and Recursive Vedic Karatsuba Multiplier Using Non-Linear Carry Select Adder. *Journal of VLSI Circuits and Systems*, 4(2), 22–29. <https://doi.org/10.31838/jvcs/04.02.04>
- [72] Btia, J., Kolba, M., Fatem, B. F., & Abbas, M. (2022). Nature's wisdom for bio-inspired printed monopole antennas. *National Journal of Antennas and Propagation*, 4(2), 13–19.
- [73] Uvarajan, K. P. (2024). Advanced modulation schemes for enhancing data throughput in 5G RF communication networks. *SCCTS Journal of Embedded Systems Design and Applications*, 1(1), 7-12. <https://doi.org/10.31838/ESA/01.01.02>
- [74] Cide, F., Arangunic, C., Urebe, J., & Revera, A. (2022). Exploring monopulse feed antennas for low Earth orbit satellite communication: Design, advantages, and applications. *National Journal of Antennas and Propagation*, 4(2), 20–27.
- [75] Vijay, V., Pittala, C. S., Koteshwaramma, K. C., Shaik, A. S., Chaitanya, K., Birru, S. G., Medapalli, S. R., & Thoranala, V. R. (2022). Design of Unbalanced Ternary Logic Gates and Arithmetic Circuits. *Journal of VLSI Circuits and Systems*, 4(1), 20–26. <https://doi.org/10.31838/jvcs/04.01.04>
- [76] David, G., Mdodo, K. L., & Kuma, R. (2022). Magnetic resonance imaging in antennas. *National Journal of Antennas and Propagation*, 4(2), 28–33.
- [77] Sudha, M., Karthikeyan, S., Daniel, J., & Muthupandian, R. (2024). Wearable device for heart rate monitoring. *International Journal of Communication and Computer Technologies*, 12(1), 27-32. <https://doi.org/10.31838/IJCCTS/12.01.03>
- [78] Mzeh, H. K., Salabi, L., Jafer, M. T., & Sikalu, T. C. (2022). Fundamentals and applications of antenna theory and design methodology. *National Journal of Antennas and Propagation*, 4(2), 34–40.

- [79] Suguna, T., Ranjan, R., Sai Suneel, A., Raja Rajeswari, V., Janaki Rani, M., & Singh, R. (2024). VLSI-Based MED-MEC Architecture for Enhanced IoT Wireless Sensor Networks. *Journal of VLSI Circuits and Systems*, 6(2), 99–106. <https://doi.org/10.31838/jvcs/06.02.11>
- [80] K. Mojail, N. Disages, H.R. Mira, H. Taconi, D. Gravino, & P.K. Nestaris (2022). Understanding capacitance and inductance in antennas. *National Journal of Antennas and Propagation*, 4(2), 41–48.
- [81] Ismail, K., & Khalil, N. H. (2025). Strategies and solutions in advanced control system engineering. *Innovative Reviews in Engineering and Science*, 2(2), 25–32. <https://doi.org/10.31838/INES/02.02.04>
- [82] Perera, M., Madugalla, A., & Chandrakumar, R. (2022). Ultra-short waves using beam transmission methodology. *National Journal of Antennas and Propagation*, 4(1), 1–7.
- [83] Rajput, A., Kumawat, R., Sharma, J., & Srinivasulu, A. (2024). Design of Novel High-Speed Energy-Efficient Robust 4:2 Compressor. *Journal of VLSI Circuits and Systems*, 6(2), 53–64. <https://doi.org/10.31838/jvcs/06.02.06>
- [84] Ulkilan, A., Mara, G. R., & Aleem, F. M. (2022). Harnessing high-temperature superconducting resonance coils and future perspectives. *National Journal of Antennas and Propagation*, 4(1), 8–13.
- [85] Pushpavalli, R., Mageshvaran, K., Anbarasu, N., & Chandru, B. (2024). Smart sensor infrastructure for environmental air quality monitoring. *International Journal of Communication and Computer Technologies*, 12(1), 33–37. <https://doi.org/10.31838/IJCCTS/12.01.04>
- [86] Pamije, L. K., Havalam, N. K., & Bosco, R. M. (2022). Challenges in wireless charging systems for implantable cardiac pacemakers. *National Journal of Antennas and Propagation*, 4(1), 14–20.
- [87] Ibrahim, N., Rajalakshmi, N. R., & Hammadeh, K. (2024). A Novel Machine Learning Model for Early Detection of Advanced Persistent Threats Utilizing Semi-Synthetic Network Traffic Data. *Journal of VLSI Circuits and Systems*, 6(2), 31–39. <https://doi.org/10.31838/jvcs/06.02.04>
- [88] Barhani, D., Kharabi, P., & Jarhoumi, E. F. (2022). The ubiquitous influence of WiMAX for next-generation applications. *National Journal of Antennas and Propagation*, 4(1), 21–26.
- [89] Sadulla, S. (2024). Next-generation semiconductor devices: Breakthroughs in materials and applications. *Progress in Electronics and Communication Engineering*, 1(1), 13–18. <https://doi.org/10.31838/PECE/01.01.03>
- [90] Zengeni, T. G., & Bates, M. P. (2022). Advancing portable telephone battery chargers with contactless electrical energy transmission systems. *National Journal of Antennas and Propagation*, 4(1), 27–32.
- [91] Pallavi, C. H., & Sreenivasulu, G. (2024). A Hybrid Optical-Acoustic Modem Based on MIMO-OFDM for Reliable Data Transmission in Green Underwater Wireless Communication. *Journal of VLSI Circuits and Systems*, 6(1), 36–42. <https://doi.org/10.31838/jvcs/06.01.06>
- [92] Chowdhury, U., & Chakma, S. (2022). Millimeter-wave technology based applications across industries. *National Journal of Antennas and Propagation*, 4(1), 33–40.
- [93] Alnumay, W. S. (2024). Use of machine learning for the detection, identification, and mitigation of cyber-attacks. *International Journal of Communication and Computer Technologies*, 12(1), 38–44. <https://doi.org/10.31838/IJCCTS/12.01.05>

- [94] Balvad, K., Lalit, D., Re-Ann, C., Halimpusan, T., & Beyes, J. O. (2022). Unveiling 4G LTE: Revolutionizing connectivity in the digital age. *National Journal of Antennas and Propagation*, 4(1), 41–46.
- [95] Klein, D., Dech, S., Raddwine, B., & Uken, E. (2023). Memory Module: High-Speed Low Latency Data Storing Modules. *Journal of VLSI Circuits and Systems*, 5(1), 35–41. <https://doi.org/10.31838/jvcs/05.01.05>
- [96] Madhusudhana Rao, K., Kishore, M. N. D., Yogesh, M. P., Saheb, S. K. A., & Hemanth, K. (2021). Triple frequency microstrip patch antenna using ground slot technique. *National Journal of Antennas and Propagation*, 3(2), 1–5.
- [97] Ariunaa, K., Tudevdağva, U., & Hussai, M. (2025). The need for chemical sustainability in advancing sustainable chemistry. *Innovative Reviews in Engineering and Science*, 2(2), 33-40. <https://doi.org/10.31838/INES/02.02.05>
- [98] Srinivasareddy, S., Narayana, Y. V., & Krishna, D. (2021). Sector beam synthesis in linear antenna arrays using social group optimization algorithm. *National Journal of Antennas and Propagation*, 3(2), 6–9.
- [99] Nuthalapati, S., Nutalapati, K., Rani, K. R., Sasirekha, L. L., Mekala, S., & Mohammad, F. P. (2021). Design of a Low Power and High Throughput 130nm Full Adder Utilizing Exclusive-OR and Exclusive-NOR Gates. *Journal of VLSI Circuits and Systems*, 3(2), 42–47. <https://doi.org/10.31838/jvcs/03.02.05>
- [100] Kesana, S., Mounika, N., Murugudu, D. S. S., Greeshma Sri, K., & Navyamadhuri, L. (2021). 24 circular and 22 rectangular microstrip patch antenna array of 4.2 GHz for satellite applications. *National Journal of Antennas and Propagation*, 3(2), 10–14.
- [101] Zorpette, G., Sengur, A., & Urban, J. E. (2023). Technological improvements in green technology and their consequences. *International Journal of Communication and Computer Technologies*, 11(2), 1-6. <https://doi.org/10.31838/IJCCTS/11.02.01>
- [102] Kesana, S., Prem Sai, N. N., Yallaiah, O., Saikrishna, S., & Khadarvali, S. (2021). Circularly polarized fractal patch antenna with probe feed technique for Wi-Max applications. *National Journal of Antennas and Propagation*, 3(2), 15–20
- [103] Rasanjani, C., Madugalla, A. K., & Perera, M. (2023). Fundamental Digital Module Realization Using RTL Design for Quantum Mechanics. *Journal of VLSI Circuits and Systems*, 5(2), 1–7. <https://doi.org/10.31838/jvcs/05.02.01>
- [104] Shaik, S. (2021). Wideband rectangular patch antenna with DGS for 5G communications. *National Journal of Antennas and Propagation*, 3(1), 1–6.
- [105] Sadulla, S. (2024). A comparative study of antenna design strategies for millimeter-wave wireless communication. *SCCTS Journal of Embedded Systems Design and Applications*, 1(1), 13-18. <https://doi.org/10.31838/ESA/01.01.03>
- [106] Singh, A. K., & Paras. (2021). Dual-beam leaky-wave antenna (LWA) based on microstrip. *National Journal of Antennas and Propagation*, 3(1), 7–10.
- [107] Srimuang, C., Srimuang, C., & Dougmla, P. (2023). Autonomous flying drones: Agricultural supporting equipment. *International Journal of Communication and Computer Technologies*, 11(2), 7-12. <https://doi.org/10.31838/IJCCTS/11.02.02>

- [108] Reddy, A. P., & Muthusamy, P. (2021). Analysis of dual-layer patch antenna for WLAN applications. *National Journal of Antennas and Propagation*, 3(1), 11–15.
- [109] Rao, K. M. K., Aneela, N. J., Sri, K. Y., Prasanna, K. N., Sahithi, N., & Likhitha, L. (2021). Design of Clocked JK Flip-Flop Using Air Hole Structured Photonic Crystal. *Journal of VLSI Circuits and Systems*, 3(2), 11–20. <https://doi.org/10.31838/jvcs/03.02.02>
- [110] Abdullah, D. (2024). Recent advancements in nanoengineering for biomedical applications: A comprehensive review. *Innovative Reviews in Engineering and Science*, 1(1), 1-5. <https://doi.org/10.31838/INES/01.01.01>
- [111] Sindhu, C. K., Sowmya, A. N., Haveela, B., & Kavya Nandini, G. (2021). Design of frequency reconfigurable microstrip antenna. *National Journal of Antennas and Propagation*, 3(1), 16–21.
- [112] Aqlan, A., Saif, A., & Salh, A. (2023). Role of IoT in urban development: A review. *International Journal of Communication and Computer Technologies*, 11(2), 13-18. <https://doi.org/10.31838/IJCCTS/11.02.03>
- [113] Kavitha, M. (2020). Wideband slotted rectangular patch antenna for short range communications. *National Journal of Antennas and Propagation*, 2(2), 1–7.
- [114] Naidu, T. M. P., Sekhar, P. C., & Boya, P. K. (2024). Low Power System on Chip Implementation of Adaptive Intra Frame and Hierarchical Motion Estimation in H.265. *Journal of VLSI Circuits and Systems*, 6(2), 40–52. <https://doi.org/10.31838/jvcs/06.02.05>
- [115] Thi Thoi, N. (2020). Dual band rectangular patch antenna with DGS for satellite communications. *National Journal of Antennas and Propagation*, 2(2), 8–14.
- [116] Sathish Kumar, T. M. (2024). Low-power design techniques for Internet of Things (IoT) devices: Current trends and future directions. *Progress in Electronics and Communication Engineering*, 1(1), 19–25. <https://doi.org/10.31838/PECE/01.01.04>
- [117] Sathwik, B., Sudha, D., Devi, Y. A. S., & Bodapati, J. (2024). RoBA Multiplier-Driven FIR Filter Synthesis: Uniting Efficiency and Speed for Enhanced Digital Signal Processing. *Journal of VLSI Circuits and Systems*, 6(2), 23–30. <https://doi.org/10.31838/jvcs/06.02.03>
- [118] Kavitha, M. (2020). A Ku band circular polarized compact antenna for satellite communications. *National Journal of Antennas and Propagation*, 2(2), 15–20.
- [119] Nam, H., Nunes, M. G. V., & Loukachevitch, N. (2023). 3D printing: Next-generation realization for future applications. *International Journal of Communication and Computer Technologies*, 11(2), 19-24. <https://doi.org/10.31838/IJCCTS/11.02.04>
- [120] Murali, D. (2020). A air cavity based multi-frequency resonator for remote correspondence applications. *National Journal of Antennas and Propagation*, 2(2), 21–26.
- [121] Pakkiraiah, C., & Satyanarayana, R. V. S. (2024). Design and FPGA Realization of Energy Efficient Reversible Full Adder for Digital Computing Applications. *Journal of VLSI Circuits and Systems*, 6(1), 7–18. <https://doi.org/10.31838/jvcs/06.01.02>
- [122] Abdullah, D. (2020). Octagonal patch quad element antenna for radar applications. *National Journal of Antennas and Propagation*, 2(2), 27–32.
- [123] Surendar, A. (2024). Emerging trends in renewable energy technologies: An in-depth analysis. *Innovative Reviews in Engineering and Science*, 1(1), 6-10. <https://doi.org/10.31838/INES/01.01.02>

- [124] Watrionthos, R. (2020). A Vivaldi antenna for 5G communications. *National Journal of Antennas and Propagation*, 2(2), 33–38.
- [125] Arora, G. K. (2024). Design of VLSI Architecture for a Flexible Testbed of Artificial Neural Network for Training and Testing on FPGA. *Journal of VLSI Circuits and Systems*, 6(1), 30–35. <https://doi.org/10.31838/jvcs/06.01.05>
- [126] Nguyen, T. D. (2020). A compact dual polarized ring slot loaded patch antenna for Navic applications. *National Journal of Antennas and Propagation*, 2(1), 1–6.
- [127] Sivaranjith, C., & Subramani, M. (2013). Development of reversible programmable gate array. *International Journal of Communication and Computer Technologies*, 1(2), 72-78. <https://doi.org/10.31838/IJCCTS/01.02.01>
- [128] Shaik, S. (2020). A coplanar waveguide fed compact antenna for navigational applications. *National Journal of Antennas and Propagation*, 2(1), 7–12.
- [129] Megha, N., Shetty, P., Kudtarkar, R. R., Naik, S. U., & Abhilash, A. L. (2024). Design and VLSI Implementation of SAR Analog to Digital Converter Using Analog Mixed Signal. *Journal of VLSI Circuits and Systems*, 6(1), 55–60. <https://doi.org/10.31838/jvcs/06.01.09>
- [130] Watrionthos, R. (2020). A compact hybrid ring patch antenna for fixed communication applications. *National Journal of Antennas and Propagation*, 2(1), 13–18.
- [131] Kumar, T. M. S. (2024). Security challenges and solutions in RF-based IoT networks: A comprehensive review. *SCCTS Journal of Embedded Systems Design and Applications*, 1(1), 19-24. <https://doi.org/10.31838/ESA/01.01.04>
- [132] Muralidharan, J. (2020). Wideband patch antenna for military applications. *National Journal of Antennas and Propagation*, 2(1), 25–30.
- [133] Bosco, K. J., Pavalam, S. M., & Mpamije, L. J. (2023). Fundamental Flip-Flop Design: Comparative Analysis. *Journal of VLSI Circuits and Systems*, 5(1), 1–7. <https://doi.org/10.31838/jvcs/05.01.01>
- [134] Puri, A., & Lakhwani, K. (2013). Enhanced approach for handwritten text recognition using neural network. *International Journal of Communication and Computer Technologies*, 1(2), 79-82. <https://doi.org/10.31838/IJCCTS/01.02.02>
- [135] Abdullah, D. (2020). A linear antenna array for wireless communications. *National Journal of Antennas and Propagation*, 2(1), 19–24.
- [136] Pittala, C. S., Sravana, J., Ajitha, G., Lakshamanachari, S., Vijay, V., & Venkateswarlu, S. C. (2021). Novel Architecture for Logic Test Using Single Cycle Access Structure. *Journal of VLSI Circuits and Systems*, 3(1), 1–6. <https://doi.org/10.31838/jvcs/03.01.01>
- [137] Kashif, R. (2019). A compact circular polarized antenna for fixed communication applications. *National Journal of Antennas and Propagation*, 1(1), 1–4.
- [138] Prasath, C. A. (2024). Cutting-edge developments in artificial intelligence for autonomous systems. *Innovative Reviews in Engineering and Science*, 1(1), 11-15. <https://doi.org/10.31838/INES/01.01.03>
- [139] Hakem, N. (2019). A compact dual frequency stacked patch antenna for IRNSS applications. *National Journal of Antennas and Propagation*, 1(1), 5–8.

- [140] Vinod, G. V., Vijendra Kumar, D., & Ramalingeswararao, N. M. (2022). An Innovative Design of Decoder Circuit Using Reversible Logic. *Journal of VLSI Circuits and Systems*, 4(1), 10–15. <https://doi.org/10.31838/jvcs/04.01.01>
- [141] Ahmed, M. I. (2019). A compact triangular ring patch antenna for radio location and fixed satellite applications. *National Journal of Antennas and Propagation*, 1(1), 9–12.
- [142] Goyal, D., Hemrajani, N., & Paliwal, K. (2013). GPH algorithm: Improved CBC improved BIFID cipher symmetric key algorithm. *International Journal of Communication and Computer Technologies*, 1(2), 83-86. <https://doi.org/10.31838/IJCCTS/01.02.03>
- [143] Yadav, N. P. (2019). A four element antenna array for amateur radio applications. *National Journal of Antennas and Propagation*, 1(1), 13–16.
- [144] Arshath, N. M. (2024). Detection of Soft Errors in Clock Synthesizers and Latency Reduction Through Voltage Scaling Mechanism. *Journal of VLSI Circuits and Systems*, 6(1), 43–50. <https://doi.org/10.31838/jvcs/06.01.07>
- [145] Kenari, M. A. (2019). Ultra wideband patch antenna for Ka band applications. *National Journal of Antennas and Propagation*, 1(1), 17–20.
- [146] Rahim, R. (2024). Adaptive algorithms for power management in battery-powered embedded systems. *SCCTS Journal of Embedded Systems Design and Applications*, 1(1), 25-30. <https://doi.org/10.31838/ESA/01.01.05>
- [147] Surendar, A., & Kavitha, M. (2019). Wideband fractal antenna for Ku band applications. *National Journal of Antennas and Propagation*, 1(1), 21–24.
- [148] Salameh, A. A., & Mohamed, O. (2024). Energy-Efficient High-Speed Quantum-Dot Cellular Automata (QCA) Based Reversible Full Adders for Low-Power Digital Computing Applications. *Journal of VLSI Circuits and Systems*, 6(2), 91–98. <https://doi.org/10.31838/jvcs/06.02.10>
- [149] Maseleno, A. (2019). Wideband rectangular patch antenna with DGS for X band applications. *National Journal of Antennas and Propagation*, 1(1), 25–28.
- [150] Shoeb, M., & Gupta, V. K. (2012). A crypt analysis of the Tiny Encryption Algorithm in key generation. *International Journal of Communication and Computer Technologies*, 1(1), 15-20. <https://doi.org/10.31838/IJCCTS/01.01.01>
- [151] Maheskumar, B. N., & Akhtar, S. (2016). An online and offline character recognition using image processing methods – A survey. *International Journal of Communication and Computer Technologies*, 4(2), 102-107.
- [152] Vijay, V., Chaitanya, K., Pittala, C. S., Ajitha, G., Susri Susmitha, S., Tanusha, J., Venkateshwarlu, S. C., & Vallabhuni, R. R. (2022). Physically Unclonable Functions Using Two-Level Finite State Machine. *Journal of VLSI Circuits and Systems*, 4(1), 33–41. <https://doi.org/10.31838/jvcs/04.01.06>
- [153] Alagu Pandian, P., Sakthivel, K., Sheik Alavudeen, K., & Lakshmi Priya, R. (2017). A low power efficient design of full adder using transmission gates. *International Journal of Communication and Computer Technologies*, 5(1), 1-5.
- [154] Kavitha, M. (2024). Embedded system architectures for autonomous vehicle navigation and control. *SCCTS Journal of Embedded Systems Design and Applications*, 1(1), 31-36. <https://doi.org/10.31838/ESA/01.01.06>

- [155] Priya, S., & Vijayan, M. (2017). Automatic street light control system using WSN based on vehicle movement and atmospheric condition. *International Journal of Communication and Computer Technologies*, 5(1), 6-11.
- [156] Mejail, M., Nestares, B. K., Gravano, L., Tacconi, E., Meira, G. R., & Desages, A. (2022). Fundamental Code Converter Block Design Using Novel CMOS Architectures. *Journal of VLSI Circuits and Systems*, 4(2), 38–45. <https://doi.org/10.31838/jvcs/04.02.06>
- [157] Velmurugan, S., & Rajasekaran, C. (2012). A reconfigurable on-chip multichannel data acquisition and processing (DAQP) system with online monitoring using network control module. *International Journal of Communication and Computer Technologies*, 1(1), 21-27. <https://doi.org/10.31838/IJCCTS/01.01.02>
- [158] Sravana, J., Indrani, K. S., Khadir, M., Saranya, M., Sai Kiran, P., Reshma, C., & Vijay, V. (2022). Realization of Performance Optimized 32-Bit Vedic Multiplier. *Journal of VLSI Circuits and Systems*, 4(2), 14–21. <https://doi.org/10.31838/jvcs/04.02.03>
- [159] Sowmiya, E., Chandrasekaran, V., & Sathya, T. (2017). Sensor node failure detection using round trip delay in wireless sensor network. *International Journal of Communication and Computer Technologies*, 5(1), 12-16.
- [160] Muralidharan, J. (2024). Innovative materials for sustainable construction: A review of current research. *Innovative Reviews in Engineering and Science*, 1(1), 16-20. <https://doi.org/10.31838/INES/01.01.04>
- [161] Rajavenkatesan, T., Mohanasundaram, C., Ajith, A. S., & Vignesh, P. (2017). Photovoltaic cooling can. *International Journal of Communication and Computer Technologies*, 5(1), 17-22.
- [162] Vikram, G. N. V. R., Navya, D., Sai Teja, Y., & Sunandini, M. (2021). Secure Home Entry with Face Recognition and Notification via Telegram. *Journal of VLSI Circuits and Systems*, 3(1), 7–13. <https://doi.org/10.31838/jvcs/03.01.02>
- [163] Duvey, A. A., Goyal, D., & Hemrajani, N. (2012). A reliable ATM protocol and comparative analysis on various parameters with other ATM protocols. *International Journal of Communication and Computer Technologies*, 1(1), 28-33. <https://doi.org/10.31838/IJCCTS/01.01.03>
- [164] Muyanja, A., Nabende, P., Okunzi, J., & Kagarura, M. (2023). Flip-Flop Realization: Conventional Memory Elements Design with Transistor Nodes. *Journal of VLSI Circuits and Systems*, 5(1), 20–27. <https://doi.org/10.31838/jvcs/05.01.03>
- [165] Gowshika, E., & Sivakumar, S. (2017). Smart LPG monitoring and controlling system. *International Journal of Communication and Computer Technologies*, 5(1), 23-26.
- [166] Rahim, R. (2024). Quantum computing in communication engineering: Potential and practical implementation. *Progress in Electronics and Communication Engineering*, 1(1), 26–31. <https://doi.org/10.31838/PECE/01.01.05>
- [167] Hrunyk, I. (2018). Computer technology applications and the data protection concept. *International Journal of Communication and Computer Technologies*, 6(1), 12-15.
- [168] Sri, R. K., Syamala, Y., Shanmukhi, S. P., Devi, P. G., & Shaik, S. (2021). Design and Performance Analysis of XOR and XNOR Functions at Low VDD Using 130nm Technology. *Journal of VLSI Circuits and Systems*, 3(1), 25–31. <https://doi.org/10.31838/jvcs/03.01.05>

- [169] Kumawat, B. (2012). A research study on packet forwarding attacks in mobile ad-hoc networks. *International Journal of Communication and Computer Technologies*, 1(1), 34-38. <https://doi.org/10.31838/IJCCTS/01.01.04>
- [170] Abbas, M. A., Hatem, T. M., Tolba, M. A., & Atia, M. (2023). Physical Design of Speed Improved Factor in FPGA Applications. *Journal of VLSI Circuits and Systems*, 5(1), 61–66. <https://doi.org/10.31838/jvcs/05.01.09>
- [171] Asadov, B. (2018). The current state of artificial intelligence (AI) and implications for computer technologies. *International Journal of Communication and Computer Technologies*, 6(1), 15-18.
- [172] Uvarajan, K. P. (2024). Advances in quantum computing: Implications for engineering and science. *Innovative Reviews in Engineering and Science*, 1(1), 21-24. <https://doi.org/10.31838/INES/01.01.05>
- [173] Usikalu, M. R., Okafor, E. N. C., Alabi, D., & Ezech, G. N. (2023). Data Distinguisher Module Implementation Using CMOS Techniques. *Journal of VLSI Circuits and Systems*, 5(1), 49–54. <https://doi.org/10.31838/jvcs/05.01.07>
- [174] Dhanalakshmi, N., Atchaya, S., & Veeramani, R. (2014). A design of multiband antenna using main radiator and additional sub-patches for different wireless communication systems. *International Journal of Communication and Computer Technologies*, 2(1), 1-5.
- [175] Kumar, C. V. S. R., & Nelakuditi, U. R. (2021). Hardware/Software Co-Design Using ZYNQ SoC. *Journal of VLSI Circuits and Systems*, 3(1), 14–18. <https://doi.org/10.31838/jvcs/03.01.03>
- [176] Onoprechuk, D. (2018). The use of computer technological simulation for designing a Cisco hierarchical framework at the Hilton Hotel. *International Journal of Communication and Computer Technologies*, 6(1), 19-22.
- [177] Abdullah, D. (2024). Leveraging FPGA-based design for high-performance embedded computing. *SCCTS Journal of Embedded Systems Design and Applications*, 1(1), 37-42. <https://doi.org/10.31838/ESA/01.01.07>
- [178] Vardhan, K. V., & Musala, S. (2024). Thermometer Coding-Based Application-Specific Efficient Mod Adder for Residue Number Systems. *Journal of VLSI Circuits and Systems*, 6(2), 122–129. <https://doi.org/10.31838/jvcs/06.02.14>
- [179] Yakubu, H. J., Aboiyar, T., & Zirra, P. B. (2018). An improved RSA image encryption algorithm using 1-D logistic map. *International Journal of Communication and Computer Technologies*, 6(1), 1-6.
- [180] Sadulla, S. (2024). State-of-the-art techniques in environmental monitoring and assessment. *Innovative Reviews in Engineering and Science*, 1(1), 25-29. <https://doi.org/10.31838/INES/01.01.06>
- [181] Jeon, S., Lee, H., Kim, H.-S., & Kim, Y. (2023). Universal Shift Register: QCA Based Novel Technique for Memory Storage Modules. *Journal of VLSI Circuits and Systems*, 5(2), 15–21. <https://doi.org/10.31838/jvcs/05.02.03>
- [182] Soni, K., Kumar, U., & Dosodia, P. (2014). A various biometric application for authentication and identification. *International Journal of Communication and Computer Technologies*, 2(1), 6-10.

- [183] Manaa Barhoumi, E., Charabi, Y., & Farhani, S. (2023). FPGA Application: Realization of IIR Filter Based Architecture. *Journal of VLSI Circuits and Systems*, 5(2), 29–35. <https://doi.org/10.31838/jvcs/05.02.05>
- [184] Yakubu, H. J., & Aboiyar, T. (2018). A chaos-based image encryption algorithm using the Shimizu-Morioka system. *International Journal of Communication and Computer Technologies*, 6(1), 7-11.
- [185] Kavitha, M. (2024). Advances in wireless sensor networks: From theory to practical applications. *Progress in Electronics and Communication Engineering*, 1(1), 32–37. <https://doi.org/10.31838/PECE/01.01.06>
- [186] Salameh, A. A., & Mohamed, O. (2024). Design and Performance Analysis of Adiabatic Logic Circuits Using FinFET Technology. *Journal of VLSI Circuits and Systems*, 6(2), 84–90. <https://doi.org/10.31838/jvcs/06.02.09>
- [187] Retheesh, D. (2014). Analysis on FPGA designs of parallel high performance multipliers. *International Journal of Communication and Computer Technologies*, 2(1), 11-18.
- [188] Marangunic, C., Cid, F., Rivera, A., & Uribe, J. (2022). Machine Learning Dependent Arithmetic Module Realization for High-Speed Computing. *Journal of VLSI Circuits and Systems*, 4(1), 42–51. <https://doi.org/10.31838/jvcs/04.01.07>
- [189] Stefanov, V. (2018). Communication technology-led development in Kenya and Sub-Saharan Africa's education systems: A cross-sectional study. *International Journal of Communication and Computer Technologies*, 6(2), 1-5.
- [190] Kumar, T. M. S. (2024). Integrative approaches in bioinformatics: Enhancing data analysis and interpretation. *Innovative Reviews in Engineering and Science*, 1(1), 30-33. <https://doi.org/10.31838/INES/01.01.07>
- [191] Koteshwaramma, K. C., Vijay, V., Bindusree, V., Kotamraju, S. I., Spandhana, Y., Reddy, B. V. D., Charan, A. S., Pittala, C. S., & Vallabhuni, R. R. (2022). ASIC Implementation of an Effective Reversible R2B FFT for 5G Technology Using Reversible Logic. *Journal of VLSI Circuits and Systems*, 4(2), 5–13. <https://doi.org/10.31838/jvcs/04.02.02>
- [192] Bala, P. M., & Ramkumar, M. O. (2014). Analyzing security of single sign-on system through advanced encryption standard. *International Journal of Communication and Computer Technologies*, 2(1), 19-28.
- [193] Tirmare, A. H., Mali, P. S., Shirolkar, A. A., Shinde, G. R., Patil, V. D., & Tirmare, H. A. (2024). VLSI Architecture-Based Implementation of Motion Estimation Algorithm for Underwater Robot Vision System. *Journal of VLSI Circuits and Systems*, 6(2), 115–121. <https://doi.org/10.31838/jvcs/06.02.13>
- [194] Perera, T. D. P. (2018). Computer network analysis in knowledge sharing. *International Journal of Communication and Computer Technologies*, 6(2), 5-8.
- [195] Surendar, A. (2024). Internet of medical things (IoMT): Challenges and innovations in embedded system design. *SCCTS Journal of Embedded Systems Design and Applications*, 1(1), 43-48. <https://doi.org/10.31838/ESA/01.01.08>
- [196] Al-Jame, F., Al-Fares, R. A., Ali, W., Ashour, H., & Murshid, N. (2023). Fundamental Design Approach: Realization of Decoder Block for Secured Transmission. *Journal of VLSI Circuits and Systems*, 5(1), 55–60. <https://doi.org/10.31838/jvcs/05.01.08>

- [197] Sundhar, C., & Archana, D. (2014). Automatic screening of fundus images for detection of diabetic retinopathy. *International Journal of Communication and Computer Technologies*, 2(1), 29-35.
- [198] Al-Yateem, N., Ismail, L., & Ahmad, M. (2023). Digital Filter-Based Adder Module Realization for High-Speed Switching Functions. *Journal of VLSI Circuits and Systems*, 5(2), 8–14. <https://doi.org/10.31838/jvcs/05.02.02>
- [199] Rajaram, A. (2018). End-user issues in the ICT industry. *International Journal of Communication and Computer Technologies*, 6(2), 9-12.
- [200] Rahim, R. (2024). Review of modern robotics: From industrial automation to service applications. *Innovative Reviews in Engineering and Science*, 1(1), 34-37. <https://doi.org/10.31838/INES/01.01.08>
- [201] Battula, B., Lakshmi, P. V., Sri, S. L. N., Karpurapu, S., & Sravya, S. D. S. (2021). Design of a Low Power and High-Speed Parity Checker Using Exclusive-OR Gates. *Journal of VLSI Circuits and Systems*, 3(2), 48–53. <https://doi.org/10.31838/jvcs/03.02.06>
- [202] Ramahrishnan, S., Elakkiya, B., Geetha, R., & Vasuki, P. (2014). Isolation enhancement in microstrip antenna arrays. *International Journal of Communication and Computer Technologies*, 2(2), 74-78. <https://doi.org/10.31838/IJCCTS/02.02.01>
- [203] Cheng, L. W., & Wei, B. L. (2023). XOR Module-Based Adder Applications Design Using QCA. *Journal of VLSI Circuits and Systems*, 5(2), 36–42. <https://doi.org/10.31838/jvcs/05.02.06>
- [204] Abdullah, D. (2024). Enhancing cybersecurity in electronic communication systems: New approaches and technologies. *Progress in Electronics and Communication Engineering*, 1(1), 38–43. <https://doi.org/10.31838/PECE/01.01.07>
- [205] Asadov, B. (2018). The current state of artificial intelligence (AI) and implications for computer technologies. *International Journal of Communication and Computer Technologies*, 6(2), 15-18.
- [206] Raj, K. Y., Vipul, G. S., Ravindra, G., Krishna, R. G. V., & Shaik, S. (2021). Design and Performance Analysis of High-Speed 8-T Full Adder. *Journal of VLSI Circuits and Systems*, 3(2), 1–10. <https://doi.org/10.31838/jvcs/03.02.01>
- [207] Chen, B. (2018). The telemedicine trend in contemporary communication technologies. *International Journal of Communication and Computer Technologies*, 6(2), 17-20.
- [208] Atia, M. (2025). Breakthroughs in tissue engineering techniques. *Innovative Reviews in Engineering and Science*, 2(1), 1-12. <https://doi.org/10.31838/INES/02.01.01>
- [209] Yuvaraj, D., Saravanakumar, G., Prasath, J. S., & Sathish Kumar, S. (2019). Design and implementation of modeling and tuning of first-order process with dead time using PID controller. *International Journal of Communication and Computer Technologies*, 7(1), 1-6.
- [210] Mukti, I. Z., Khan, E. R., & Biswas, K. K. (2024). 1.8-V Low Power, High-Resolution, High-Speed Comparator with Low Offset Voltage Implemented in 45nm CMOS Technology. *Journal of VLSI Circuits and Systems*, 6(1), 19–24. <https://doi.org/10.31838/jvcs/06.01.03>
- [211] Malar Tamil Prabha, I., & Gayathri, R. (2014). Isolation enhancement in microstrip antenna arrays. *International Journal of Communication and Computer Technologies*, 2(2), 79-84. <https://doi.org/10.31838/IJCCTS/02.02.02>

- [212] Chakma, K. S., & Chowdhury, M. S. U. (2023). CSA Implementation Using Novel Methodology: RTL Development. *Journal of VLSI Circuits and Systems*, 5(2), 22–28. <https://doi.org/10.31838/jvcs/05.02.04>
- [213] Monisha, S., Monisha, M., Deepa, P., & Sathya, R. (2019). An android application for exhibiting statistical chronicle information. *International Journal of Communication and Computer Technologies*, 7(1), 7-9.
- [214] Prasath, C. A. (2024). Energy-efficient routing protocols for IoT-enabled wireless sensor networks. *Journal of Wireless Sensor Networks and IoT*, 1(1), 1-7. <https://doi.org/10.31838/WSNIOT/01.01.01>
- [215] Malathi, K., Dhivya, E., Monisha, M., & Pavithra, P. (2019). Preterm birth prognostic prediction using cross-domain data fusion. *International Journal of Communication and Computer Technologies*, 7(1), 10-13.
- [216] Bodapati, J., Sudahkar, O., & Karthik Raju, A. G. V. (2022). An Improved Design of Low-Power High-Speed Accuracy Scalable Approximate Multiplier. *Journal of VLSI Circuits and Systems*, 4(1), 7–11. <https://doi.org/10.31838/jvcs/04.01.02>
- [217] Sakthive, V., Kesaven, P. V., Martin William, J., & Madan Kumar, S. K. (2019). Integrated platform and response system for healthcare using Alexa. *International Journal of Communication and Computer Technologies*, 7(1), 14-22.
- [218] Thoi, N. T. (2025). Nanoparticle applications revolutionizing chemical processes. *Innovative Reviews in Engineering and Science*, 2(1), 13-21. <https://doi.org/10.31838/INES/02.01.02>
- [219] Zakaria, R., & Mohd Zaki, F. (2023). Digital Filter Design: Novel Multiplier Realization. *Journal of VLSI Circuits and Systems*, 5(2), 43–49. <https://doi.org/10.31838/jvcs/05.02.07>
- [220] Abinaya, R., Abinaya, R., Vidhya, S., & Vadivel, S. (2014). Latent palm print matching based on minutiae features for forensic applications. *International Journal of Communication and Computer Technologies*, 2(2), 85-87. <https://doi.org/10.31838/IJCTS/02.02.03>
- [221] Lofandri, W., Selvakumar, C., Sah, B., Sangeetha, M., & Beulah Jabaseeli, N. (2024). Design and Optimization of a High-Speed VLSI Architecture for Integrated FIR Filters in Advanced Digital Signal Processing Applications. *Journal of VLSI Circuits and Systems*, 6(1), 70–77. <https://doi.org/10.31838/jvcs/06.01.12>
- [222] Saranya, U., & Madhubala, P. (2019). Enhancement of security and network lifetime using flexi-cast method. *International Journal of Communication and Computer Technologies*, 7(1), 23-26.
- [223] Al-Yateem, N., Ismail, L., & Ahmad, M. (2024). A comprehensive analysis on semiconductor devices and circuits. *Progress in Electronics and Communication Engineering*, 2(1), 1–15. <https://doi.org/10.31838/PECE/02.01.01>
- [224] Manon Mary, A., Bhuvaneswar, M., Haritha, N., Krishnaveni, V., & Punithavathisivathanu, B. (2019). Design of automatic number plate recognition system for moving vehicle. *International Journal of Communication and Computer Technologies*, 7(1), 1-5.
- [225] Ariunaa, K., Tudevdagva, U., & Hussai, M. (2023). FPGA-Based Digital Filter Design for Faster Operations. *Journal of VLSI Circuits and Systems*, 5(2), 56–62. <https://doi.org/10.31838/jvcs/05.02.09>

- [226] Jamuna, K., Jayapriya, G., & Jayanthi, K. (2014). MEMS-based haptic assistive system for physical impairments. *International Journal of Communication and Computer Technologies*, 2(2), 88-93. <https://doi.org/10.31838/IJCCTS/02.02.04>
- [227] Devi, K. G., Tejasree, K., Sri, M. K. S., & Pravallika, M. (2021). Energy Reduction of D-Flipflop Using 130nm CMOS Technology. *Journal of VLSI Circuits and Systems*, 3(2), 34–41. <https://doi.org/10.31838/jvcs/03.02.04>
- [228] Karunya, L. C., Harini, P., Iswarya, S., & Jerlin, A. (2019). Emergency alert security system for humans. *International Journal of Communication and Computer Technologies*, 7(1), 6-10.
- [229] Danh, N. T. (2025). Advanced geotechnical engineering techniques. *Innovative Reviews in Engineering and Science*, 2(1), 22-33. <https://doi.org/10.31838/INES/02.01.03>
- [230] Sudhakar, R., Rajakumari, J., Poornima, S., & Ramya, V. (2019). A security threats and authentication approaches in wireless sensor networks. *International Journal of Communication and Computer Technologies*, 7(2), 1-3.
- [231] Kondam, R. R., Sekhar, P. C., & Boya, P. K. (2024). Low Power SoC-Based Road Surface Crack Segmentation Using UNet with EfficientNet-B0 Architecture. *Journal of VLSI Circuits and Systems*, 6(1), 61–69. <https://doi.org/10.31838/jvcs/06.01.11>
- [232] Jeevanand, D., Keerthivasan, K., Mohamed Rilwan, J., & Murugan, P. (2014). Real-time embedded network video capture and SMS alerting system. *International Journal of Communication and Computer Technologies*, 2(2), 94-97. <https://doi.org/10.31838/IJCCTS/02.02.05>
- [233] Rao, M. K. M., Bharadwaj, P. V. N. S., Vali, S. M., Mahesh, N., & Sai, T. T. (2021). Design of Clocked Hybrid (D/T) Flip-Flop Through Air Hole Paradigm Photonic Crystal. *Journal of VLSI Circuits and Systems*, 3(2), 21–33. <https://doi.org/10.31838/jvcs/03.02.03>
- [234] Santhi, D., Kumar, N., Kumar, G., Mohandoss, S., & Venkatasubramanian, R. (2019). Quantum-Dot Cellular Automata based public key cryptography. *International Journal of Communication and Computer Technologies*, 7(2), 13-18.
- [235] Velliangiri, A. (2024). Security challenges and solutions in IoT-based wireless sensor networks. *Journal of Wireless Sensor Networks and IoT*, 1(1), 8-14. <https://doi.org/10.31838/WSNIOT/01.01.02>
- [236] Devi, M. R., Rajameenakshi, S., Vignesh, S., & Mukesh Raj, M. (2019). Rope climbing bot. *International Journal of Communication and Computer Technologies*, 7(2), 19-21.
- [237] Juma, J., Mdodo, R. M., & Gichoya, D. (2023). Multiplier Design Using Machine Learning Algorithms for Energy Efficiency. *Journal of VLSI Circuits and Systems*, 5(1), 28–34. <https://doi.org/10.31838/jvcs/05.01.04>
- [238] Ristono, A., & Budi, P. (2025). Next-gen power systems in electrical engineering. *Innovative Reviews in Engineering and Science*, 2(1), 34-44. <https://doi.org/10.31838/INES/02.01.04>
- [239] Karthik, R., Miruthula, A., & Nitheeswari, N. (2019). Web-based online machine controlling and monitoring using PLC via Modbus communication. *International Journal of Communication and Computer Technologies*, 7(2), 22-26.
- [240] Sreenivasu, M., Kumar, U. V., & Dhulipudi, R. (2022). Design and Development of Intrusion Detection System for Wireless Sensor Network. *Journal of VLSI Circuits and Systems*, 4(2), 1–4. <https://doi.org/10.31838/jvcs/04.02.01>

- [241] Dhanalakshmi, N., Atchaya, S., & Veeramani, R. (2015). A design of multiband antenna using main radiator and additional sub-patches for different wireless communication systems. *International Journal of Communication and Computer Technologies*, 3(1), 1-5. <https://doi.org/10.31838/IJCCTS/03.01.01>
- [242] Mejail, M., Nestares, B. K., & Gravano, L. (2024). The evolution of telecommunications: Analog to digital. *Progress in Electronics and Communication Engineering*, 2(1), 16–26. <https://doi.org/10.31838/PECE/02.01.02>
- [243] Kiruthika, J., Poovizhi, V., Kiruthika, P., Madura, E., & Narmatha, P. (2019). Blockchain-based unforgeable license. *International Journal of Communication and Computer Technologies*, 7(2), 4-7.
- [244] Kulkarni, S., & Ravi, J. N. (2024). Smart Ways to Catch the Abutment DRCs at IP Level. *Journal of VLSI Circuits and Systems*, 6(1), 51–54. <https://doi.org/10.31838/jvcs/06.01.08>
- [245] Ibrahim, R. (2020). Workstation Cluster's Hadoop Distributed File System Simulation and Modeling. *International Journal of Communication and Computer Technologies*, 8(1), 1-4.
- [246] Zain, Z. (2025). Exploring the field of mechatronics: Scope and future. *Innovative Reviews in Engineering and Science*, 2(1), 45-51. <https://doi.org/10.31838/INES/02.01.05>
- [247] Wickramasinghe, K. (2020). The Use of Deep Data Locality towards a Hadoop Performance Analysis Framework. *International Journal of Communication and Computer Technologies*, 8(1), 5-8.
- [248] Snousi, H. M., Aleej, F. A., Bara, M. F., & Alkilany, A. (2022). ADC: Novel Methodology for Code Converter Application for Data Processing. *Journal of VLSI Circuits and Systems*, 4(2), 46–56. <https://doi.org/10.31838/jvcs/04.02.07>
- [249] Venkatesh Guru, K. (2015). Active low energy outlay routing algorithm for wireless ad hoc network. *International Journal of Communication and Computer Technologies*, 3(1), 5-8. <https://doi.org/10.31838/IJCCTS/03.01.02>
- [250] Kabasa, B., Chikuni, E., Bates, M. P., & Zengeni, T. G. (2023). Data Conversion: Realization of Code Converter Using Shift Register Modules. *Journal of VLSI Circuits and Systems*, 5(1), 8–19. <https://doi.org/10.31838/jvcs/05.01.02>
- [251] Vishegurov, S. K. (2020). VANET Communication Range Degradation: An Experimental Study on the Role of Interference 2.0. *International Journal of Communication and Computer Technologies*, 8(1), 9-12.
- [252] Muralidharan, J. (2024). Machine learning techniques for anomaly detection in smart IoT sensor networks. *Journal of Wireless Sensor Networks and IoT*, 1(1), 15-22. <https://doi.org/10.31838/WSNIOT/01.01.03>
- [253] Murodov, S. S. (2020). Examining DoD's Implementation of FITARA and the Implication for IT-Based Defense Systems: A U.S. Case Study. *International Journal of Communication and Computer Technologies*, 8(1), 13-16.
- [254] Van, C., Trinh, M. H., & Shimada, T. (2023). Next-Generation Semiconductor-Based Fundamental Computation Module Implementation. *Journal of VLSI Circuits and Systems*, 5(2), 50–55. <https://doi.org/10.31838/jvcs/05.02.08>
- [255] Baros, D. K. (2020). Evaluating the Efficacy of Using Computerized Shifting Information Systems (NCSIS) in organizations – Towards Effective and Computer Technology-Based

- Administration. *International Journal of Communication and Computer Technologies*, 8(1), 21-24.
- [256] Sathish Kumar, T. M. (2024). Developing FPGA-based accelerators for deep learning in reconfigurable computing systems. *SCCTS Transactions on Reconfigurable Computing*, 1(1), 1-5. <https://doi.org/10.31838/RCC/01.01.01>
- [257] Papalou, A. (2023). Proposed Information System towards Computerized Technological Application – Recommendation for the Acquisition, Implementation, and Support of a Health Information System. *International Journal of Communication and Computer Technologies*, 8(2), 1-4.
- [258] Zakaria, R., & Zaki, F. M. (2024). Vehicular ad-hoc networks (VANETs) for enhancing road safety and efficiency. *Progress in Electronics and Communication Engineering*, 2(1), 27–38. <https://doi.org/10.31838/PECE/02.01.03>
- [259] Keliwar, S. (2023). A Secondary Study Examining the Effectiveness of Network Topologies: The Case of Ring, Bus, and Star Topologies. *International Journal of Communication and Computer Technologies*, 8(2), 5-7.
- [260] Sadulla, S. (2024). Techniques and applications for adaptive resource management in reconfigurable computing. *SCCTS Transactions on Reconfigurable Computing*, 1(1), 6-10. <https://doi.org/10.31838/RCC/01.01.02>
- [261] Annapurna, K., Deepthi, K., & Seetha Ramajanyelu, B. (2021). Comparison of soft fusion techniques for cooperative spectrum sensing in cognitive radio networks. *International Journal of Communication and Computer Technologies*, 9(1), 1-5.
- [262] Ramanan, S. V., & Vimal, E. (2015). Minimizing the energy consumption of wireless sensor network by comparing the performances of maxweight and minimum energy scheduling algorithms. *International Journal of Communication and Computer Technologies*, 3(1), 9-15. <https://doi.org/10.31838/IJCCTS/03.01.03>
- [263] Uvarajan, K. P. (2024). Integration of blockchain technology with wireless sensor networks for enhanced IoT security. *Journal of Wireless Sensor Networks and IoT*, 1(1), 23-30. <https://doi.org/10.31838/WSNIOT/01.01.04>
- [264] Ponduri, V., & Mohan, L. (2021). Reliable multiple object detection on noisy images by using Yolov3. *International Journal of Communication and Computer Technologies*, 9(1), 6-9.
- [265] Rahim, R. (2024). Optimizing reconfigurable architectures for enhanced performance in computing. *SCCTS Transactions on Reconfigurable Computing*, 1(1), 11-15. <https://doi.org/10.31838/RCC/01.01.03>
- [266] Surendheran, A. R., & Prashanth, K. (2015). A survey of energy-efficient communication protocol for wireless sensor networks. *International Journal of Communication and Computer Technologies*, 3(2), 50-57. <https://doi.org/10.31838/IJCCTS/03.02.01>
- [267] Barhoumi, E. M., Charabi, Y., & Farhani, S. (2024). Detailed guide to machine learning techniques in signal processing. *Progress in Electronics and Communication Engineering*, 2(1), 39–47. <https://doi.org/10.31838/PECE/02.01.04>
- [268] Srinivasu, L. N., & Veeramani, V. (2021). Curve-let transform based text-in-image steganography using Huffman coding. *International Journal of Communication and Computer Technologies*, 9(1), 10-14.

- [269] Kavitha, M. (2024). Enhancing security and privacy in reconfigurable computing: Challenges and methods. *SCCTS Transactions on Reconfigurable Computing*, 1(1), 16-20. <https://doi.org/10.31838/RCC/01.01.04>
- [270] Kalaiyarasi, V., & Tamilarasi, M. (2015). Survey of load balancing routing protocols in MANET. *International Journal of Communication and Computer Technologies*, 3(2), 58-62. <https://doi.org/10.31838/IJCCTS/03.02.02>
- [271] Sadulla, S. (2024). Optimization of data aggregation techniques in IoT-based wireless sensor networks. *Journal of Wireless Sensor Networks and IoT*, 1(1), 31-36. <https://doi.org/10.31838/WSNIOT/01.01.05>
- [272] Annapurna, K., & Yesaswini, A. M. (2021). Improved Hungarian algorithm for unbalanced assignment problems. *International Journal of Communication and Computer Technologies*, 9(1), 27-33.
- [273] Abdullah, D. (2024). Strategies for low-power design in reconfigurable computing for IoT devices. *SCCTS Transactions on Reconfigurable Computing*, 1(1), 21-25. <https://doi.org/10.31838/RCC/01.01.05>
- [274] R.T., Yamine, & N.S., Nithya. (2015). Survey on high utility itemset mining. *International Journal of Communication and Computer Technologies*, 3(2), 63-66. <https://doi.org/10.31838/IJCCTS/03.02.03>
- [275] Madugalla, A. K., & Perera, M. (2024). Innovative uses of medical embedded systems in healthcare. *Progress in Electronics and Communication Engineering*, 2(1), 48-59. <https://doi.org/10.31838/PECE/02.01.05>
- [276] Surendar, A. (2024). Survey and future directions on fault tolerance mechanisms in reconfigurable computing. *SCCTS Transactions on Reconfigurable Computing*, 1(1), 26-30. <https://doi.org/10.31838/RCC/01.01.06>
- [277] Balamurugan, R., & Nagarajan, N. R. (2017). Automatic robotic arm using hand gestures. *International Journal of Communication and Computer Technologies*, 5(2), 43-45.
- [278] Kumar, T. M. S. (2024). Low-power communication protocols for IoT-driven wireless sensor networks. *Journal of Wireless Sensor Networks and IoT*, 1(1), 37-43. <https://doi.org/10.31838/WSNIOT/01.01.06>
- [279] S, A. Spoorthi, T. D. Sunil, & Kurian, M. Z. (2021). Implementation of LoRa-based autonomous agriculture robot. *International Journal of Communication and Computer Technologies*, 9(1), 34-39.
- [280] Jagan, B. O. L. (2024). Low-power design techniques for VLSI in IoT applications: Challenges and solutions. *Journal of Integrated VLSI, Embedded and Computing Technologies*, 1(1), 1-5. <https://doi.org/10.31838/JIVCT/01.01.01>
- [281] Mahendran, S., Benita, R., Nandhini, S., & Nandhitha, J. (2017). Fault detection in power transmission line. *International Journal of Communication and Computer Technologies*, 5(2), 46-47.
- [282] Cheng, L. W., & Wei, B. L. (2024). Transforming smart devices and networks using blockchain for IoT. *Progress in Electronics and Communication Engineering*, 2(1), 60-67. <https://doi.org/10.31838/PECE/02.01.06>

- [283] Geetha, K. (2024). Advanced fault tolerance mechanisms in embedded systems for automotive safety. *Journal of Integrated VLSI, Embedded and Computing Technologies*, 1(1), 6-10. <https://doi.org/10.31838/JIVCT/01.01.02>
- [284] Rohini, S., Sharanya, M., Vidhya, A., Viji, S., & Poornima, P. (2017). Proximity coupled microstrip antenna for Bluetooth, WIMAX, and WLAN applications. *International Journal of Communication and Computer Technologies*, 5(2), 48-52.
- [285] Rahim, R. (2024). Scalable architectures for real-time data processing in IoT-enabled wireless sensor networks. *Journal of Wireless Sensor Networks and IoT*, 1(1), 44-49. <https://doi.org/10.31838/WSNIOT/01.01.07>
- [286] RANGISETTI, R., & ANNAPURNA, K. (2021). Routing attacks in VANETs. *International Journal of Communication and Computer Technologies*, 9(2), 1-5.
- [287] Prasath, C. A. (2024). Optimization of FPGA architectures for real-time signal processing in medical devices. *Journal of Integrated VLSI, Embedded and Computing Technologies*, 1(1), 11-15. <https://doi.org/10.31838/JIVCT/01.01.03>
- [288] Gopalakrishnan, K., Lakshmanan, R., Naveen, V., TamilKumaran, S., & Venkatesh, S. (2017). Digital signature manager. *International Journal of Communication and Computer Technologies*, 5(2), 53-57.
- [289] Ali, W., Ashour, H., & Murshid, N. (2025). Photonic integrated circuits: Key concepts and applications. *Progress in Electronics and Communication Engineering*, 2(2), 1-9. <https://doi.org/10.31838/PECE/02.02.01>
- [290] Kavitha, M. (2024). Energy-efficient algorithms for machine learning on embedded systems. *Journal of Integrated VLSI, Embedded and Computing Technologies*, 1(1), 16-20. <https://doi.org/10.31838/JIVCT/01.01.04>
- [291] Pradeep, M., Abinya, R., Sathya Anandhi, S., & Soundarya, S. (2017). Dynamic smart alert service for women safety system. *International Journal of Communication and Computer Technologies*, 5(2), 58-66.
- [292] Kavitha, M. (2024). Environmental monitoring using IoT-based wireless sensor networks: A case study. *Journal of Wireless Sensor Networks and IoT*, 1(1), 50-55. <https://doi.org/10.31838/WSNIOT/01.01.08>
- [293] ASIF, M., BARNABA, M., RAJENDRA BABU, K., OM PRAKASH, P., & KHAMURUDEEN, S. K. (2021). Detection and tracking of theft vehicle. *International Journal of Communication and Computer Technologies*, 9(2), 6-11.
- [294] Muralidharan, J. (2023). Innovative RF design for high-efficiency wireless power amplifiers. *National Journal of RF Engineering and Wireless Communication*, 1(1), 1-9. <https://doi.org/10.31838/RFMW/01.01.01>
- [295] Sundararaju, K., & Sukumar, P. (2016). Improvement of power quality using PQ theory-based series hybrid active power filter. *International Journal of Communication and Computer Technologies*, 4(2), 59-63.
- [296] Abdullah, D. (2024). Design and implementation of secure VLSI architectures for cryptographic applications. *Journal of Integrated VLSI, Embedded and Computing Technologies*, 1(1), 21-25. <https://doi.org/10.31838/JIVCT/01.01.05>

- [297] Srilakshmi, K., Preethi, K., Afsha, M., Pooja Sree, N., & Venu, M. (2022). Advanced electricity billing system using Arduino Uno. *International Journal of Communication and Computer Technologies*, 10(1), 1-3.
- [298] Sathish Kumar, T. M. (2023). Wearable sensors for flexible health monitoring and IoT. *National Journal of RF Engineering and Wireless Communication*, 1(1), 10-22. <https://doi.org/10.31838/RFMW/01.01.02>
- [299] Rajesh Kumar, B., & Jayaprakash, R. (2016). Harmonic mitigation in doubly fed induction generator for wind conversion systems by using integrated active filter capabilities. *International Journal of Communication and Computer Technologies*, 4(2), 64-71.
- [300] Van, C., Trinh, M. H., & Shimada, T. (2025). Graphene innovations in flexible and wearable nanoelectronics. *Progress in Electronics and Communication Engineering*, 2(2), 10–20. <https://doi.org/10.31838/PECE/02.02.02>
- [301] Arunabala, C., Brahmateja, G., Raju, K., Gideon, K., & Venkateswar Reddy, B. (2022). GSM adapted electric lineman safety system with protection based circuit breaker. *International Journal of Communication and Computer Technologies*, 10(1), 4-6.
- [302] Rahim, R. (2023). Effective 60 GHz signal propagation in complex indoor settings. *National Journal of RF Engineering and Wireless Communication*, 1(1), 23-29. <https://doi.org/10.31838/RFMW/01.01.03>
- [303] Sudhir, M., Maneesha, K., Anudeepthi, G., Anusha, T., & Chandini, A. (2022). Untangling Pancard by designing optical character reader tool box by correlating alphanumeric character. *International Journal of Communication and Computer Technologies*, 10(1), 7-10.
- [304] Santhosh, M., Kavitha, S., Keerthana, R., Suganya, L., & Krishnakumar, S. (2016). Electronic voting machine using internet. *International Journal of Communication and Computer Technologies*, 4(2), 72-75.
- [305] Arvinth, N. (2024). Integration of neuromorphic computing in embedded systems: Opportunities and challenges. *Journal of Integrated VLSI, Embedded and Computing Technologies*, 1(1), 26-30. <https://doi.org/10.31838/JIVCT/01.01.06>
- [306] Suneetha, J., Venkateshwar, C., Rao, A.T.V.S.S.N., Tarun, D., Rupesh, D., Kalyan, A., & Sunil Sai, D. (2023). An intelligent system for toddler cry detection. *International Journal of Communication and Computer Technologies*, 10(2), 5-10.
- [307] Kavitha, M. (2023). Beamforming techniques for optimizing massive MIMO and spatial multiplexing. *National Journal of RF Engineering and Wireless Communication*, 1(1), 30-38. <https://doi.org/10.31838/RFMW/01.01.04>
- [308] Venkatesh, N., Suresh, P., Gopinath, M., & Rambabu Naik, M. (2023). Design of environmental monitoring system in farmhouse based on Zigbee. *International Journal of Communication and Computer Technologies*, 10(2), 1-4.
- [309] Kumar, D. S., & Veeramani, R. (2016). Harvesting microwave signal power from the ambient environment. *International Journal of Communication and Computer Technologies*, 4(2), 76-81.
- [310] Muyanja, A., Nabende, P., Okunzi, J., & Kagarura, M. (2025). Metamaterials for revolutionizing modern applications and metasurfaces. *Progress in Electronics and Communication Engineering*, 2(2), 21–30. <https://doi.org/10.31838/PECE/02.02.03>

- [311] Prasath, C. A. (2023). The role of mobility models in MANET routing protocols efficiency. National Journal of RF Engineering and Wireless Communication, 1(1), 39-48. <https://doi.org/10.31838/RFMW/01.01.05>
- [312] Nandhini, P., Vijayasharathy, G., Kokila, N. S., Kousalya, S., & Kousika, T. (2016). An improved approach of DWT and ANC algorithm for removal of ECG artifacts. International Journal of Communication and Computer Technologies, 4(2), 82-87.
- [313] Usikalu, M. R., Alabi, D., & Ezech, G. N. (2025). Exploring emerging memory technologies in modern electronics. Progress in Electronics and Communication Engineering, 2(2), 31–40. <https://doi.org/10.31838/PECE/02.02.04>
- [314] Veerappan, S. (2023). Designing voltage-controlled oscillators for optimal frequency synthesis. National Journal of RF Engineering and Wireless Communication, 1(1), 49-56. <https://doi.org/10.31838/RFMW/01.01.06>
- [315] Devi, G., Reena, P., Yuvarani, M., Kavitha, M., & Surendar, A. (2016). High-speed image searching for human gait feature selection. International Journal of Communication and Computer Technologies, 4(2), 88-95.
- [316] Chakma, K. S. (2025). Flexible and wearable electronics: Innovations, challenges, and future prospects. Progress in Electronics and Communication Engineering, 2(2), 41–46. <https://doi.org/10.31838/PECE/02.02.05>