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# Design of a High speed Low Low-Power Latched Comparator for Medical Implants

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**Abstract:**

The latched dynamic comparator is a fundamental component in all ADC architectures. Thermal effects, kickback, and offset voltage influence it. The kickback noise of the latched comparator in medical implant ADCs can impact the resolution, precision, and settling period. The current study examines a latching comparator that aims to reduce kickback noise. This research presents a low-power latched comparator for medical implants functioning at 1 V. This investigation implements a comparator utilising the sampling switching approach. This method successfully minimises kick-back noise and clocking feed-through by minimising unwanted charge injections in the comparator. The comparator decreases power usage while maintaining noise levels. The comparator uses 45-nanometre CMOS technology. The proposed comparator demonstrates superior performance compared to leading comparators regarding kickback noise, power consumption, delay. The input voltage has an inverse effect on the comparator's delay. Simulations indicate that the comparator uses 31 nW at 1 V. The comparator consumes 70% less power compared with different systems. The suggested sample modification decreases kickback noise by a minimum of 18%.

**Keywords:** Latched Comparator, medical implants, ADC architectures, , CMOS 45nm technology, power delay product (PDP)

## 1. INTRODUCTION

The semiconductor field is presently experiencing significant expansion, attributed to its unique circuitry, which offers solutions for a wide range of expected applications. Modern applications that interact with external environments exhibit a range of frequency variations. Numerous electronic circuits integrate a conventional analog monitoring block, which poses difficulties for signal storing due to the analogue nature of the input and output signals.

Contemporary electronic devices require conversion devices to transform analogue signals onto digital signals, enabling the transfer and storage of digital data. The electronics sector generally store electrical signals in an analogue way. Certain devices utilise sensors to identify signals emitted from an individual's body or additional devices, eventually transforming the observed signals to electrical outputs. The growing demand for modern technologies that minimise power usage has rendered the advancement of CMOS-based concepts essential. The requirement for handheld electronic devices is substantial, attributed to their ability for recording and analysing biopotential signals [3].

The schematic representation of a bio-signal acquisition mechanism is presented in Figure 1. A sensor acquires a physical input signal, subsequently amplifying and filtering it to generate a digital output. The oscillator generates a signal called a clock that enhances the analogue input signals in an ADC, leading to a digitised result. As a result, the transmitting element emits the produced digital signal as its result [4,5].

Several ADC frameworks have recently become accessible in the industry. The selection of a suitable ADC remains essential, as it significantly impacts the performance of handheld devices such as healthcare equipment, heart rate monitors, and wireless networks of sensors. The SAR-ADC has been recognised as an effective ADC due to its operation at a direct-current voltage, provision of precise measurements, low power consumption, and small chip dimensions, as indicated in sources [7, 8].

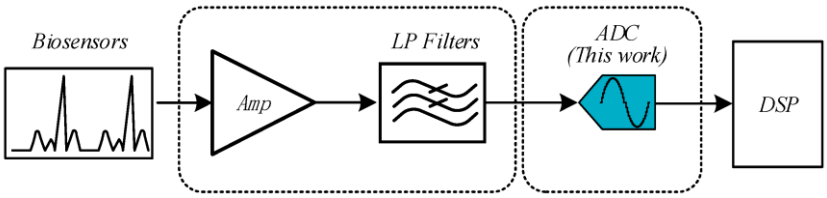



Figure 1: Analog Front End for Bio-medical applications

The comparator has become an integral component of all ADCs.

The comparator serves as the primary component for energy usage analysis within SAR-ADC design structures pertinent to biological purposes. As a result, SAR ADCs require comparators that exhibit minimal power use and minimised chip dimensions. An innovative implementation pertains to implanted medical equipment . The growing prevalence of battery-operated devices requires the incorporation of low-power devices , resulting in a heightened use of dynamic latched comparators. The resultant separation enables independent regulation of speed, energy use. Therefore, prior studies [5-8] indicate that a comparator requires both high bandwidth and speed. Latch comparators have gained increased popularity over static comparators within low-power medical applications. The integration of positive feedback, as opposed to a static comparator, facilitates a faster charging process of the resultant node, as demonstrated in reference [8]. Reference [9] indicates that the decrease in transistor dimensions has resulted in an escalation of static power loss within the latch-type voltage detecting amplifier. The operation of stacked devices necessitates considerable voltage space, which poses a challenge for scaled CMOS technology . The common-mode voltage upon the input significantly influences sensitivity in terms of both speed alongside offset throughout this framework [10]. This feature renders it unsuitable for physiological tasks that necessitate deviations in input voltage of common mode. Achieving a high-performance conception necessitates positioning the positive feedback phase of the latch away from the inputs to operate.

The focus of the current study is the development of a double-tail comparator, highlighting its ability to facilitate a reduced quantity of stacked transistors. Previous studies [9, 11] demonstrate that this characteristic makes it suitable for tasks requiring minimal voltage, lower energy usage, and improved speed performance. The division of the amplification as well latch stages enables the use of minimal tail current within the amplification phase while allowing for substantial current within the latch phase.

This configuration leads to minimal offset and enhanced speed, as detailed in references [9, 12]. As the velocity increases and power dissipation decreases, there is a corresponding increase in both offset and kickback noise. The design of dynamic latching comparators is significantly influenced by these considerations. The implementation of a lower offset necessitates the employment of larger transistors, which leads to an increase in parasitic capacitance, a deceleration in the regeneration process, and an escalation in power dissipation, as evidenced by previous studies [10, 11, 13]. The input-referred offset voltage of a precise dynamic latch comparator determines its key attributes concerning power consumption, speed, and dimensions. The main objective of this study is to improve the design of a latching comparator with respect to energy consumption and switching speed. The comparator has been calibrated for optimal performance within a specified supply voltage range of 350 millivolts to 1 volt. Additionally, it has been designed to function reliably at clock frequencies ranging from 50 to 200 kilohertz. It is important to note that this specific application does not solely determine the configuration of the comparator. The optimal performance of the comparator may vary based on the specific operational area being analysed, with the objective of enhancing power efficiency and minimising delay time. Extensive scholarly literature documents the utilisation of latched sense amplifiers in conjunction with regenerative comparators, highlighting their capabilities in delivering rapid decision-making, minimising power consumption, and achieving satisfactory accuracy [11–14]. The reduction of static leakage current leads to decreased energy consumption, while the provision of strong positive feedback facilitates an exceptionally rapid response.
Section 2 outlines the traditional comparators, however Section 3 details the methodology and its execution of the recommended comparator. Section 4 of this study presents the findings from the simulation, while Section 5 offers the concluding remarks.

## 2. Conventional Double Tail Comparator

Modern biomedical systems require the integration of low-voltage, low-powered gadgets in the design of circuits. Eliminating the pre-amplification stage can optimise energy usage, area, and delay in a system. This method improves the system's efficiency. The removal of the pre-amplification stage leads to decreased power consumption and reduced area requirements. This section discusses various types of dynamic latched comparators.

Figure 2 presents the architectural representation or circuit diagram of a single-tail dynamic comparator. The operation of the framework is divided into two separate phases, each dependent on the clocking signal (CLK). Whenever the CLK has reached a low state ('0'), the comparator can continue to function throughout the reset stage. According to the circumstances specified, device N1 remains in a non-conductive state, leading to the lack of a pathway for discharge from its outputs to ground. Furthermore, given that devices P1 and P4 are within a conducting state, the voltage that comes out generated by the comparator is projected to be nearly equal to Vdd. When the CLK signal attains an appropriate high state associated with VDD, the comparator commences the comparison stage.

According to the circumstances described, device N1 will exhibit an active state, signifying the establishment of a discharging pathway that carries the comparator outcomes to the ground. The resultant discharge rate depends on the voltages found within the input transistors of the comparator, specifically N2 along with N3.

The gate ports of each of these transistors are connected to the Vinn alongside Vinp ports, correspondingly. Reference [13] states that when Vinn surpasses Vinp, the discharge rate of outcome Voutn will be greater compared to the rate of outcome Voutp, and vice versa.

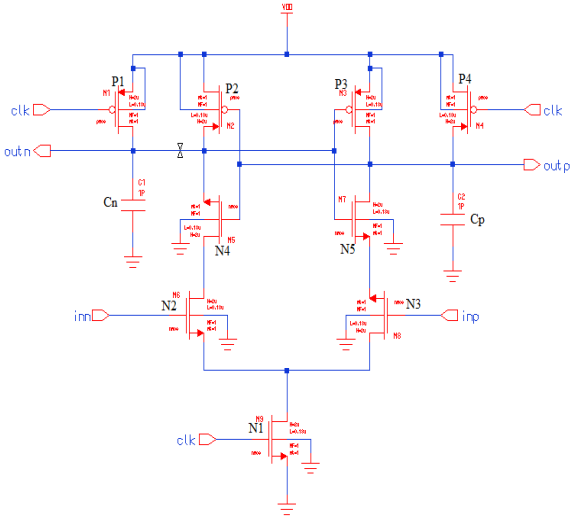



Figure 2: Schematic representation of single tail comparator

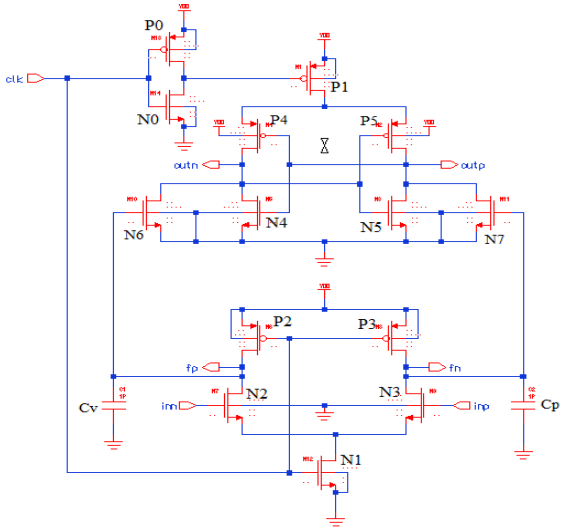



Figure 3: Schematic representation of Double tail Comparator

The CMOS latched comparators referenced in the investigation underwent simulation utilising CMOS 45nm technological advancements. Figures 4 and 5 present the transient modelling responses for single and double tail latched comparators, correspondingly. When the CLK has reached a low state, the resultant nodes, referred to simply as Outp and Outn, have been observed charging to an acceptable voltage equal to VDD. Whenever the CLK has reached a high state, the resultant node Outn discharges to ground if VINN surpasses VINP. The process of charging of the resultant node Outp towards VDD occurs in the opposite manner.

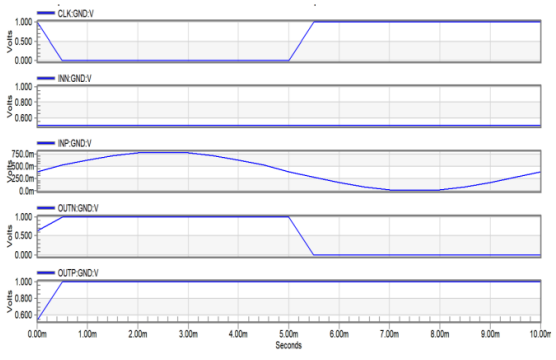



Figure 4: Transient computational outcome of single tail comparator

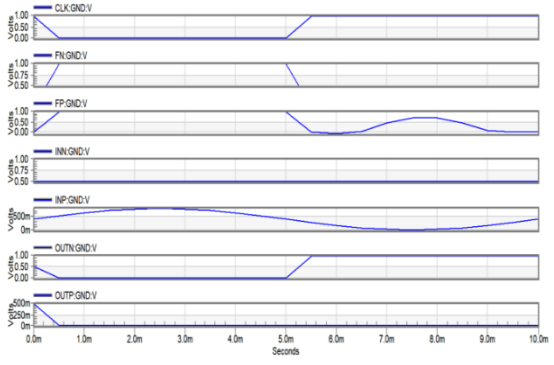



Figure 5: Transient computational outcome of double tail comparator

The double tail comparator architectural design exhibits reduced tracking compared to the conventional single tail comparator. The use of a double tail configuration facilitates a substantial current flow throughout the assessment stage, resulting in a reduction of offset, as indicated in previous studies [15, 16].

The delay of the comparator is defined as the time taken for the output differential signal to reach VDD/2. The total delay introduced by the comparator is comprised of two primary aspects: the delay correlated with the latch, stemming from the cross-coupled inverting latches ( M7/M8, M5/M6), and the delay linked to the charging of the resultant load capacitance till the primary NMOS transistor (M7/M8) engages [17,18].

The typical double tail comparator's total delay may be expressed analytically as follows:

$$t_{delay} = t_0 + t_{latch} \quad (1)$$

$$t_0 = \frac{V_{THN} C_{out}}{I_p} = \frac{2V_{THN} C_{out} u_p C_{ox} \frac{W_p}{L_p}}{g_{mP}^2} \quad (2)$$

Where in $u_p -$ mobility of holes, $V_{THN}$–threshold voltages of the transistors N4 and N5,

Ip- current through P4, Cout - load capacitance of the comparator output nodes, $g_{mp}$-P4 transistor's transconductance , Lp , Wp are lengths and widths of transistor P4 respectively.

The time delay associated with the latch can be determined using Equation (3), which is provided below:

$$t_{latch} = \frac{C_L}{g_{m,eff}} . \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right)$$

$$= \frac{C_L}{g_{m,eff}} . \ln\left(\frac{V_{dd}/2}{\Delta V_0}\right) \quad (3)$$

ΔV0 constitutes a variable that represents the variation in the latch's initial voltage at the output at the commencement of the regeneration procedure. Throughout the evaluation, both of the cross-coupled inverters remains within the ON state. As a result, the total effective transconductance can be calculated using the following method:

$$t_{delay} = \frac{2V_{THN} C_{out} u_p C_{ox} \frac{W_p}{L_p}}{g_{mP}^2} \ldots + \frac{C_L}{g_{m,eff}} . \ln\left(\frac{V_{dd}/2}{\Delta V_0}\right) \quad (4)$$

The functional delay that occurs in the comparator is notably influenced by the capacitive loads present at the latching output nodes, fluctuations within the input voltage, and the trans-conductance (gm) associated with both the input and temporary transistors, as illustrated in Equation (4). A reduction in latency is caused by an increase in ΔV0.

## 3. Proposed Latched Comparator

### A. Description of the circuit

Various methodologies are available for the development of the comparator. Latched comparators exhibit enhanced performance relative to alternative comparators through the optimisation of multiple parameters, including speed, power, and offset voltage.

The design incorporates enhanced isolation of input and output , minimises kickback noise, and has been optimised for low-voltage functions. A dynamic latched comparator has been designed for biomedical devices characterised by low power consumption and minimal kickback noise.

The schematic diagram of the proposed comparator utilising the kickback noise mitigation approach is illustrated in Figure 6. The analysis of the existing literature indicates that the proposed comparator effectively addresses the problem of clock feed through. The solution involves the integration of an NMOS transistor, designated as M12, positioned between the clock input signal and the tail transistor of the comparator, M11. This configuration ensures that the tail transistor is not directly linked to the clock input. The gate terminal of the M12 transistor is permanently connected to Vdd, resulting in the transistor being in an always ON state. Additionally, while the source terminal of transistor M12 is linked to the clock, its drain terminal is connected to transistor M11. This configuration leads to a notable clock delay and effectively mitigates the clock feed-through issue. In CMOS 45nm technology, the design and simulation of the required circuitry are conducted using Mentor Graphics tools.

The dynamic comparator is designed to operate as outlined below: The suggested comparator functions through two distinct methodologies: a evaluation mode and a resetting procedure. During the reset or recharging phase, when the clock has reached zero, the devices M7-M8 and M12, which are designated for kickback noise reduction, are disabled to prevent static power consumption in the circuitry. The M3 and M4 devices are engaged during this operational phase, leading to a short circuit in Vdd and affecting the associated nodes of the comparator.

Consequently, Vdd has been connected to the outcomes of the Comparator, specifically Out-P along with Out-n.

The resultant nodes of the proposed comparator become disconnected from its input nodes whenever the deices M7 alongside M8, utilised for kickback noise mitigation, are deactivated. The function of devices M9 and M10, that are are linked to the input signals, is not affected by the two outcomes of the latch.

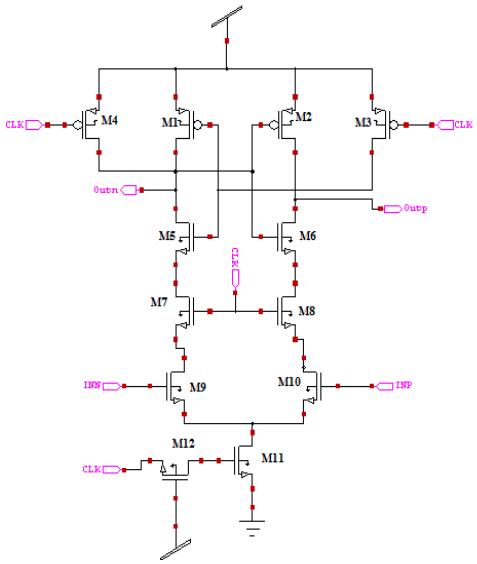



Figure 6: Architecture of Proposed kickback noise reduced Comparator

In the assessment stage, the clock signal has been assigned to VDD (CLK=VDD). The tail transistor M11, along with M3 and M6, remain in the off state, whereas the devices utilised for Kickback noise elimination are activated. Devices M7 along with M8 become operational to mitigate kickback noise.

The input differential voltage generated is routed to cross-coupled inverter-dependent latches, which then perform the required decision-making process.

Furthermore, both of the outputs of the comparator, OutP alongside Out-n, begin to discharging the voltage at varying rates, influenced by the distinct input voltages applied to the devices M9-M10, as well as the tail transistor M11. When the incoming voltage at INN exceeds that at INP, the voltage at the resultant terminal Out-P decreases more rapidly than the voltage at the node that produces the signal Outn, and conversely. The output terminal Out-P exhibits an accelerated method for |Vdd-Vth| when contrasted with different terminals. The regenerating process of invertering latches ( M2-M6,M1-M5 ) results in the continued activation of the corresponding PMOS device M1. The result of Out-n is therefore equivalent to Vdd. The output signal OutP has been determined to be 0 due to the functioning capability of the PMOS device M2. The main benefit of the recommended comparator conceptualisation is the requirement for only one regulating clock signal. This removes the need for synchronisation between the various control signals, thus improving the effectiveness of the circuitry.

The proposed circuitry facilitates most effective delay and power elimination. The tail device features a small form factor, facilitating the delivery of the necessary lower tail current for the operation of the differentiating input transistor stage.

The elimination of the requirement for extra transistors within the configuration or restoring of the circuitry results in a reduction of circuit complexities. In the regeneration phase, it becomes crucial to isolate the drains of the transistors that constitute the input component of the differential conjunction from any regeneration nodes that are connected

This measure is implemented to prevent the formation of kickback noise, that is initiated by fluctuations at the regenerating nodes. In order to accomplish this duty, switching devices M7 and M8 must be used to integrate the regenerative node and the input component of the differential pair's drains.

These switches prejudiced for operation in strong an inversion may have been designed with an increased size to attain a higher transconductance, thus reducing the effects of thermal noise. Consequently, the regenerating node and every drain of the input section of the differential pair suffer from a lack of isolation at the start of the regeneration process.

The development process integrates tailored transistor sizing alongside matching approaches to minimise offset voltage, thereby addressing the impacts of a mismatch and fabrication variability.

## B. DESIGNING FACTORS

When the proposed Comparator is implemented, the following design elements are carried out.

### Region of Operation

The present design employs the subthreshold operating zone of MOSFETs to achieve a reduction in supply voltage and power utilisation. The progression of comparators in ultra-deepeer sub-micrometer CMOS technology encounters obstacles owing to insufficient supply voltages.

This issue arises primarily from the insufficient corresponding scaling between the the minimum acceptable voltages of these devices and the source voltages utilised in modern CMOS processes [19]. Consequently, the challenge of designing comparators escalates as the source voltage diminishes.

The analysis focusses on a comprehensive all-regional framework referred to as the "EKV Model," which examines the operational viability of transistors within an inversion region. The described framework is employed to enhance Comparator noise and power, as outlined in references [22-25]. The following equations related to the MOS device are utilised for the calculation of the EKV configuration.

$$IC = \frac{I_D}{I_S} \tag{6}$$

$$I_s = 2\,\mu C_{ox} \frac{W}{L} \emptyset_t^2 \tag{7}$$

Where,

$I_D$ - Drain Current

IC - Inversion Coefficient.

$I_S$ - Normalization current

$\eta$ - slope factor.

$C_{ox}$- Capacitance of the oxide layer,

$t_{ox}$- thickness of oxide layer,

$\phi_t$- Thermal voltage at room temperature.

In the present investigation, the coefficient of IC has been chosen at 0.1, which guarantees that the transistors operate throughout the weak inversion area. The physical dimensions of the transistor have been established based on this methodology.

Several design considerations require thorough evaluation throughout the development process of the proposed comparator. This framework is characterised by the presence of a cross-coupled latching device and the corresponding switches, M5 along with M6. During the assessment stage, it is essential to activate the M5 alongside M6 switches whereas simultaneously reducing the voltage from the source to the drain of the specified switches. The complete discharging of its resultant nodes has become critically important in this scenario.

Therefore, a collection of nMOS transistors which are regulated by an amplified voltage are utilised. The control voltage had been determined to be VDD + 0.3 volts.

The load capacitance encompasses the parasitic capacitance of M5 as well M6, thereby requiring a meticulous equilibrium among switch-on resistance alongside parasitic capacitance. Figure 7 depicts the delay as well as power use of the comparator under consideration, as influenced by the different widths of switches M5 and M6. While the overall width of M5,6 surpasses 250nm, increasing the width is not going to contribute to a significant decrease in delay but instead leads to increased power consumption. Therefore, it was determined that the width of M5,6 is smaller than 250nm.

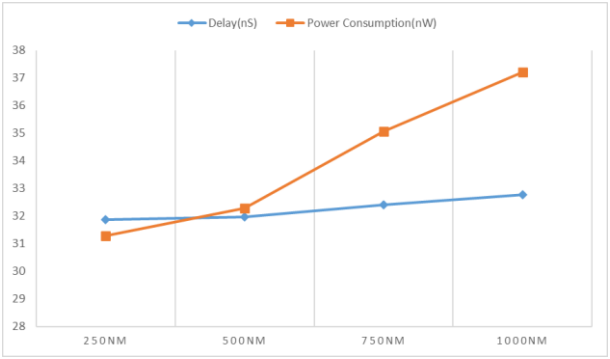



Figure 7: The comparative analysis of the simulated delay as well as power use of the proposed comparator with respect to the varying widths of switches M5 as well as M6.

The transistor sizes within the comparator are calculated according to the EKV approach, as illustrated in Table 1.

Table 1 suggested transistor dimensions for the comparator

| **Transistor** | **ratio of W/L** |
|---|---|
| M1-M2-M4 | 2/1 |
| M10- M9-M8- M7- M6- M5 | 4/1 |
| M12- M11 | 8/1 |

**Kickback noise**

At the onset of the regenerating stage, the switching device is disengaged, prompting both cross-coupled inverting devices to start generating positive feedback. The outputs' voltages converge towards 0 and VDD, consistent with the minimal output voltage that is observed at the conclusion of the resetting stage. Furthermore, the impact on the inner capacitances of MOS devices, along with the imbalance in transistors, possesses the potential to worsen the current scenario.

The variation in the input voltage may affect the accuracy of the converter. The disruption described above is typically known as kickback noise, according to reference [29]. Higher speed comparators generally produce an increased level of kickback noise. During the pre-charging stage, the differential input voltage becomes enhanced without interference, since the regeneration procedure has not commenced, as noted in reference [10].

During the very beginning of the comparative stage, the auxiliary transistors M7-8 are turned on to facilitate the starting of the decision-making and following regenerating procedure, as indicated in reference [30]. The transistors operating in the triode region are configured in parallel via the input differential pair transistors, which contributes to the reduction of fluctuations in voltage at the drain terminal of the input transistor. This leads to a decrease in the formation of kickback noise.

The proposed comparator demonstrated a decreased level of kickback noise as a result of the incorporation of auxiliary devices M7 and M8. The implementation of these transistors was designed to isolate the output nodes, thus reducing the influence of mismatch effects alongside the parasitic capacitance related to the transistors throughout the device design process. As a result, the reduction of offset in the feedback loop was achieved by properly sizing transistors to function within the weaker inversion area and enhancing for mismatches.

**Analysis of Delay in Proposed Comparator**

A mathematical statement has been developed to show the influence of different design factors on the functionality of the dynamic comparator [25, 26]. The suggested comparator delay consists of two delays, i.e. discharge delay $t_o$ & latch delay $t_{latch..}$ The discharge delay defines the duration for which the load capacitance discharges as long as the PMOS transistor corresponding to the latch remains activated.

When INP exceeds INN, the current of an input transistor having INP as input forces the output terminal $Out_p$ to drain much faster than the output terminal Out-$_n$ . As a result, the discharge delay can be represented as

$$t_0 = \frac{C_L|V_{thp}|}{I_{current\ in\ the\ INP\ transistor}} \cong 2\frac{C_L|V_{thp}|}{I_{\ current\ present\ in\ \ tail\ transistor}} \quad (22)$$

$$I_{current\ at\ the\ INP\ transistor} = \frac{I_{\ current\ present\ \ in\ the\ \ tail\ transistor}}{2} + \Delta I_{in} = \frac{I_{\ current\ in\ tail\ transistor}}{2} + g_{m(input\ transistors)} \quad (23)$$

$$I_{M10} = \frac{I_{M11}}{2} + \Delta I_{in} = \frac{I_{M11}}{2} + g_{m9,10}$$

Where $\Delta I_{in}$– variations associated with the input differential voltage.

The $t_{latch}$ delay is produced by the latch delay inherent in both cross-coupled inverterting latches. Consider the voltage swing to be Vdd which is derived from the differential input voltage.

$$t_{latch} = \frac{C_L}{g_{m,eff}} . ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right)$$

$$= \frac{C_L}{g_{m,eff}} . ln\left(\frac{V_{dd}}{\Delta V_0}\right) \quad (24)$$

Where,$t_{latch}\frac{C_L}{g_{m,eff}}$ –latch transconductance.

In dynamic Comparator, $\Delta V_0$is written as

$$\Delta V_0 = \left|V_{outp}(t = t_0) - V_{outn}(t = t_0)\right|$$

$$= \left|V_{thp}\right| - \frac{I_{INP}t_0}{C_L} = \left|V_{thp}\right|\left(1 - \frac{I_{INP}}{I_{INN}}\right) \quad (25)$$

The difference current $\Delta I_{in=}|\ I_{INN} - I_{INP}|$ is relatively too small than the other individual currents. Where, $I_{INP}$- Current is flowing through the transistor with an input voltage designated as INP.

, $I_{INN}$- Current is flowing through the transistor with an input voltage designated as INN.

Thus, INN will be $\frac{I\ current\ flowing\ through\ all\ the\ \ tail\ transistor}{2}$ and can be written as

$$\Delta V_0 = \left|V_{thp}\right|\frac{\Delta I_{in}}{I_{INN}} \quad (26)$$

$$\approx 2\left|V_{thp}\right|\frac{\Delta I_{in}}{I_{tail}}$$

$$= 2\left|V_{thp}\right|\frac{\sqrt{\beta_{inputtransistors}I_{tail}}}{I_{tail}}\Delta V_{in}$$

$$= 2\left|V_{thp}\right|\sqrt{\frac{\beta_{inputtransistors}}{I_{tail}}}\Delta V_{in}$$

Where, $\beta_{inputtransistors}$- the present value of input transistors

,$I_{tail}$- current in tail transistor. Keeping $\Delta V_0$ value within the expression of latch delay. The cumulative delay could be outlined outlined below

$$td = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}}.\ln\left(\frac{V_{DD}}{2|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right) \quad (27)$$

$$td = 2\frac{C_L|V_{thp}|}{I_{M11}} + \frac{C_L}{g_{m,eff}}.\ln\left(\frac{V_{DD}}{2|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{M11}}{\beta_{1,2}}}\right) \quad (28)$$

The influence of different design factors on total delay time may be observed in (28). This investigation indicates that the delay time of the recommended comparator is typically proportional to the load capacitance CL of the comparator and inversely dependent on the differential voltage ΔV_in across the two inputs to operate.

According to equation 27, delayed discharging with reduced $I_{tail}$ current results in an increase in the onset difference voltage $\Delta V_o$ by decreasing the$t_{latch}$.

## 4. SIMULATION RESULTS

A comparative analysis of the proposed comparator and existing comparators was conducted through simulations on all circuits utilising 45 nm CMOS technology. The parameters included a Vdd of 1 V, a differential voltage of Vdiff = 30 mV, and a CLK frequency of 1 GHz, employing Mentor Graphics software tools for the analysis. The simulation result corresponding to this analysis is presented in Figure 10. The output terminals of the comparator are connected to Vdd when the CLK signal is at a logic level of '0.' When the CLK is configured to logic '1,' the output of the comparator, OUT-P, generates a value of zero, while OUT-N outputs Vdd when the condition INP>INN is met. Conversely, when INP

The comparators had been optimised and the physical dimensions of the transistors were adjusted to achieve a consistent offset standard deviation of 0.5 V at the input common mode voltage. Table 2 provides a succinct summary of the results obtained for various parameters related to the proposed comparator. In contrast, Table 3 presents an assessment of performance metrics, including delay, power consumption, and PDP, for the frameworks mentioned in relation to the proposed comparator. Table 3 presents the percentage improvement with regard to the aforementioned elements for the proposed comparator architecture, as compared to the comparator architectures mentioned earlier.

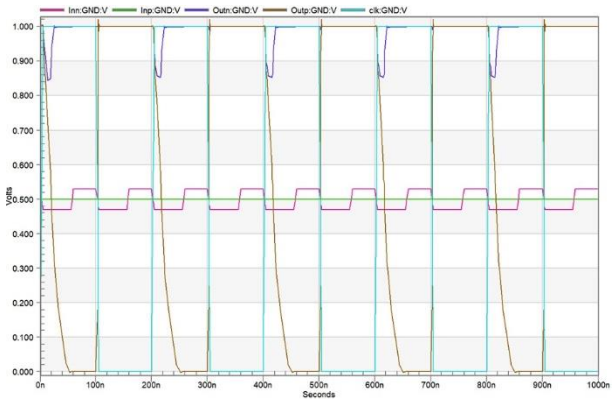



Figure 10: Transient Simulation of Proposed Comparator

Table 2: Performance of the proposed comparator

| Parameter for the simulation | Value |
|---|---|
| Source voltage | 1V |
| CMOS technology | 45nm |
| Operational frequency | 1GHz |
| Power utilization | 31.2 nW |
| Offset voltage | 7.52 mV |
| Delay | 31.9 nS |
| Power delay product (PDP) | 0.996 fJ |
| Kickback Noise | 0.3 mV |

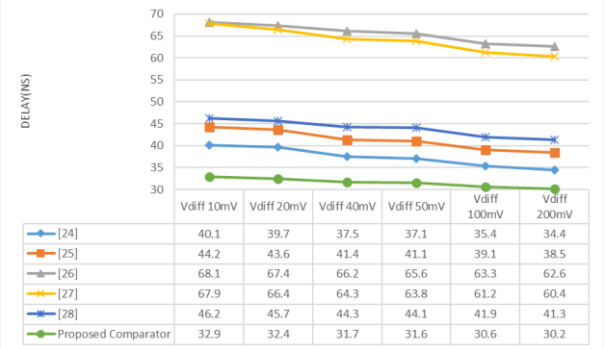
Table 3: Analysis of the recommended comparator in relation to conventional comparators

| **Comparator Properties** | **[24]** | **[ 25]** | **[26]** | **[27]** | **[28]** | **Proposed comparator** |
|---|---|---|---|---|---|---|
| Power dissipation (nW) | 31.45 | 59.87 | 57.43 | 85.93 | 59.57 | 31.29 |
| Delay (ns) | 38.64 | 42.54 | 67.12 | 65.34 | 45.23 | 31.86 |
| Kickback noise (mV) | 1.4 | 0.87 | 1.3 | 1.24 | 1.81 | 0.29 |
| Offset voltage(μV) | 8.8 | 7.8 | 7.73 | 12.5 | 13.7 | 7.52 |
| Power Delay Product (fW/S ) | 1.215 | 2.54 | 3.85 | 5.614 | 2.69 | 0.996 |

The results of the pre-layout modelling for Power, delay of the recommended comparator, as well as the referenced comparator, with respect to the input differential voltage, are illustrated in Figures 11 and 12, correspondingly.

As evidenced by the data presented in Figure 11, the delay exhibited by the proposed comparator is comparatively lower than that of other referenced comparators across the entire range of input differential voltage. In accordance with the findings presented in Figure 12, it is evident that the power levels remain consistently minimal across all ranges. Within double tail present configurations, the comparator delay typically exhibits reduced sensitivity to deviations in input common-mode voltage relative to the traditional dynamic structure. The former demonstrates a broader common-mode spectrum. The study models the proposed comparator to analyse its variables as an outcome of input

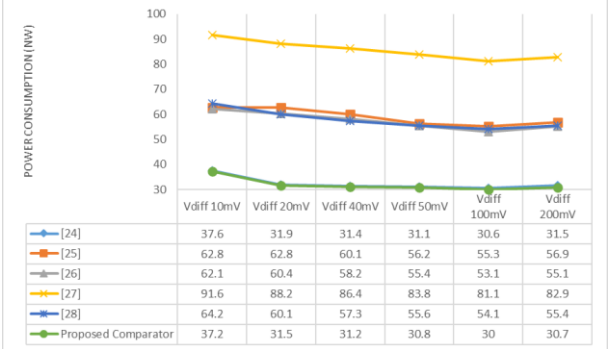
differential voltage through various common-mode voltages, using a Vdd of 1 V and a clock speed of 1 GHz.




| | Vdiff 10mV | Vdiff 20mV | Vdiff 40mV | Vdiff 50mV | Vdiff 100mV | Vdiff 200mV |
|---|---|---|---|---|---|---|
| [24] | 40.1 | 39.7 | 37.5 | 37.1 | 35.4 | 34.4 |
| [25] | 44.2 | 43.6 | 41.4 | 41.1 | 39.1 | 38.5 |
| [26] | 68.1 | 67.4 | 66.2 | 65.6 | 63.3 | 62.6 |
| [27] | 67.9 | 66.4 | 64.3 | 63.8 | 61.2 | 60.4 |
| [28] | 46.2 | 45.7 | 44.3 | 44.1 | 41.9 | 41.3 |
| Proposed Comparator | 32.9 | 32.4 | 31.7 | 31.6 | 30.6 | 30.2 |

Figure 11: Delay of the recommended comparator concerning input voltage difference

(Vdiff)



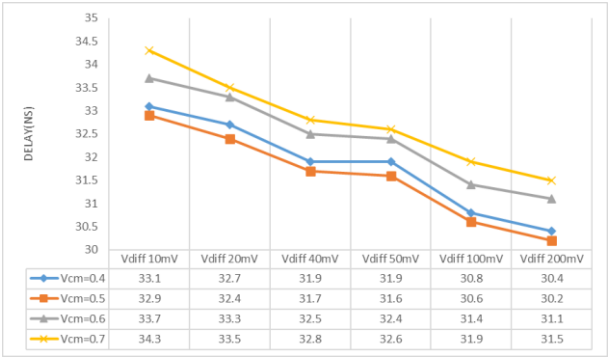

| | Vdiff 10mV | Vdiff 20mV | Vdiff 40mV | Vdiff 50mV | Vdiff 100mV | Vdiff 200mV |
|---|---|---|---|---|---|---|
| [24] | 37.6 | 31.9 | 31.4 | 31.1 | 30.6 | 31.5 |
| [25] | 62.8 | 62.8 | 60.1 | 56.2 | 55.3 | 56.9 |
| [26] | 62.1 | 60.4 | 58.2 | 55.4 | 53.1 | 55.1 |
| [27] | 91.6 | 88.2 | 86.4 | 83.8 | 81.1 | 82.9 |
| [28] | 64.2 | 60.1 | 57.3 | 55.6 | 54.1 | 55.4 |
| Proposed Comparator | 37.2 | 31.5 | 31.2 | 30.8 | 30 | 30.7 |

Figure 12: Power Consumption of the recommended comparator concerning input voltage difference

(Vdiff)

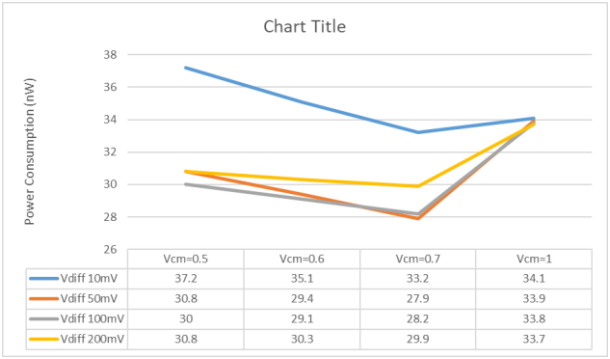
Figure 13 provides an illustration that illustrates the relationship between the delay time of the comparator in question as well as the variation in input voltage levels for various supply voltages. At a designated VDD with 1 V, the delay has been determined as 32.85 ns with an input differential voltage level of ΔVin equal to ten mV.

The observed delay exhibits a reduction from 32.9 nanoseconds to 30.7 nanoseconds as the input voltage difference (ΔVin) ranges from 10 millivolts to 200 millivolts. Figure 13 illustrates the simulated delay of the comparator as an outcome of input differential voltage, considering multiple common-mode voltage values. The delay remains consistent at an acceptable level and shows similarity throughout its input common-mode voltage that ranges from 0.4-0.7 V. As the variation in the differential input voltage drops, the delay reduces.The influence of common-mode voltage, represented as Vcm, on power loss across various ΔVin values had been Simulated, with the results illustrated in Figure 14. This finding indicates that the loss of power decreases as the level of Vcm increases from 0.5 to 1 V, given a particular value regarding ΔVin. Whenever the Vcm swing varies between 0.7 to 1 V, a rise in power usage becomes apparent, although it remains lower compared to that recorded for the previous amplitude. Whenever the input voltage variability (ΔVin) has been 10 mV, the power usage declines from 37.2 W with an input common-mode voltage (Vcm) concerning 0.5 V to 34.1 nW at a Vcm with 1 V. Figure 14 illustrates that the comparator in question demonstrates a decreased dependence on Vcm due to the absence of static power loss.




| | Vdiff 10mV | Vdiff 20mV | Vdiff 40mV | Vdiff 50mV | Vdiff 100mV | Vdiff 200mV |
|---|---|---|---|---|---|---|
| Vcm=0.4 | 33.1 | 32.7 | 31.9 | 31.9 | 30.8 | 30.4 |
| Vcm=0.5 | 32.9 | 32.4 | 31.7 | 31.6 | 30.6 | 30.2 |
| Vcm=0.6 | 33.7 | 33.3 | 32.5 | 32.4 | 31.4 | 31.1 |
| Vcm=0.7 | 34.3 | 33.5 | 32.8 | 32.6 | 31.9 | 31.5 |

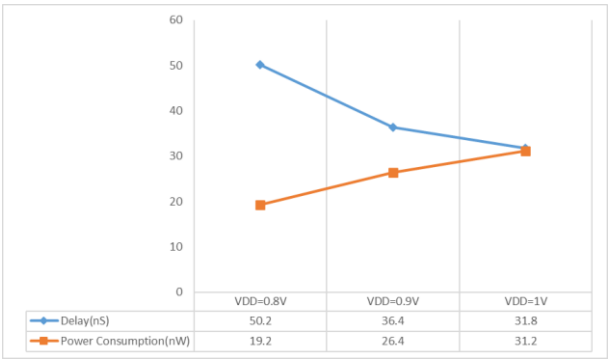
Figure 13: Delay of the recommended comparator versus input voltage difference (Vdiff) at various common-mode voltage (Vcm) levels with Vdd set to 1 V and CLK at 1 GHz.




| | Vcm=0.5 | Vcm=0.6 | Vcm=0.7 | Vcm=1 |
|---|---|---|---|---|
| Vdiff 10mV | 37.2 | 35.1 | 33.2 | 34.1 |
| Vdiff 50mV | 30.8 | 29.4 | 27.9 | 33.9 |
| Vdiff 100mV | 30 | 29.1 | 28.2 | 33.8 |
| Vdiff 200mV | 30.8 | 30.3 | 29.9 | 33.7 |

Figure 14: Power Consumption of the proposed comparator Vs input voltage difference (Vdiff) using Vcm values at Vdd = 1 V, CLK = 1 GHz

The simulation analyses the effects of varying supply voltages on power consumption and latency, with the results shown in Figure 15. The chart illustrates a definitive correlation between supply voltage and the resultant delay, signifying that an increase in power supply results in a reduction in delay.




| | VDD=0.8V | VDD=0.9V | VDD=1V |
|---|---|---|---|
| Delay(nS) | 50.2 | 36.4 | 31.8 |
| Power Consumption(nW) | 19.2 | 26.4 | 31.2 |

Figure 15: Power Consumption & delay Vs.various supply voltages at Vcm = 0.5 V, CLK = 1 GHz

Figure 16 depicts the standard variation corresponding to the offset for the comparator suggested in this research, which is measured at 7.5 mV, based on the computational results obtained. The data was obtained by performing Monte Carlo calculations with 300 samples.

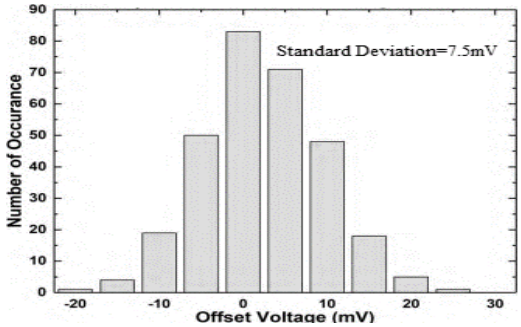



Figure 16: Monte Carlo analysis of Offset for 300 Samples

To assess the efficacy of the proposed comparator, computations were conducted prior to following the arrangement for both the conventional and suggested designsCareful consideration was applied to the organisation of elements to reduce effects on the comparator's delay and power consumption.

Figure 17 depicts the design concepts of the proposed comparator. Table 3 presents a comparative analysis of the simulation outcomes acquired prior to and following the layout modification. The results demonstrate that the expected area requirement of the recommended comparator remains either equivalent or minimal in total when VDD=1V, Vcm=0.5V, and Vdiff=30mV.

Table 3: Overview of the efficiency of the comparators

| **Properties of the Comparator** | | **STDLC** | **DTDLC** | **Recommended comparator** |
|---|---|---|---|---|
| Power utilization (nW) | Pre-Layout | 31.45 | 59.87 | 31.29 |
| | Post - Layout | 34.76 | 67.28 | 32.97 |
| Delay (ns) | Pre-Layout | 38.64 | 42.54 | 31.86 |
| | Post - Layout | 42.76 | 49.44 | 36.54 |
| Area | | 3.63µm X 4.1µm | 3.7µm X 4.2µm | 3.6µm X 4.12µm |

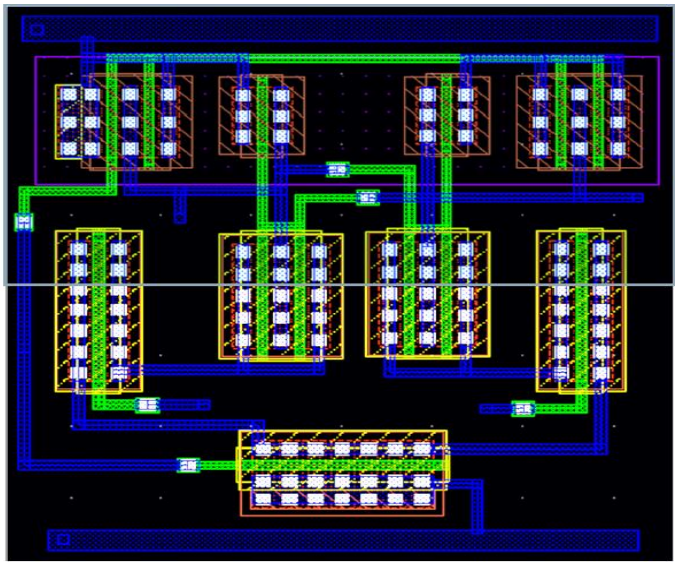


Figure 17: Layout of proposed comparator

As technological advances shrinks and fabrication complexity increases, it is essential to replicate comparators across different process corners. Figure 18 depicts an examination of the impacts of process corner modifications on power usage ,delay for the suggested comparator along with the comparator under reference.

The results validate that the effectiveness metrics of the comparator being analysed demonstrate negligible variability throughout all process corners.

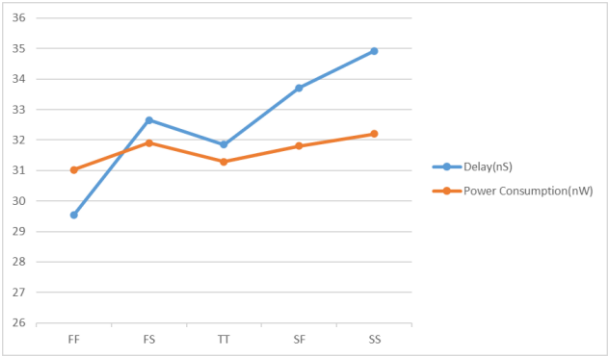



Figure 18: Evaluation of process corner variability in delay along with power usage for the recommended comparator in comparison to referenced comparators.

Figure 19 highlights the temperature's impact on the recommended comparator's delay as well as power usage. According to Figure 7, the power usage of the suggested Comparator is directly related to temperature and delay is inversely proportional to temperature.

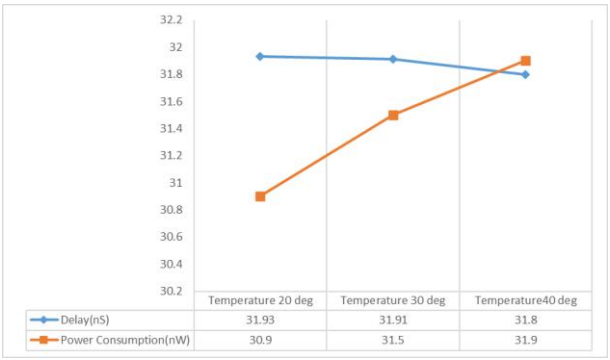



Figure 19: Variation of Power Consumption and Delay w.r.t temperature at VDD=1V, Vdiff=30mV, Vcm=0.5V

## 5. Conclusion

The present investigation presents a comprehensive analysis of a low-power, high-speed, low-kickback noise latched comparator designed for biological applications. This research employed 45nm CMOS semiconductor technology utilising a voltage source of 1 volt. The proposed comparator employs a sampling switching method to mitigate kickback distortion. In both comparison and reset phases, the proposed comparator does not require extra devices for result configuration. The latency of the comparator exhibits an inverse correlation between its differential and common-mode inputs.

A comparison investigation was performed to assess the functional attributes of the recommended comparator against the current standards in comparator designing. The suggested comparator consumes a minimum of 72% less power than previous models. Additionally, the suggested kickback noise approach, which integrates a sampling switching into the specified architecture, minimises kickback noise by a minimum of 18%. Simulation findings indicate that the latency of the suggested

comparator has been inversely related to its input voltage. Subsequently, the performance features of the proposed comparator are evaluated concerning different input parameters.

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