Communications on Applied Nonlinear Analysis
ISSN: 1074-133X
Vol 32 No. 1s (2025)

Enhancing Low Energy Technology Performance: Optimizing Low Noise Amplifier through Stabilization and Input-Output Component Matching Design

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Article History:
Received: *19-08-2024*
Revised: *01-10-2024*
Accepted: *19-10-2024*

Abstract:
Advancements in technology, marked by increased miniaturization, integration, and accessibility, have propelled the widespread adoption of CMOS technology in wireless applications. This trend has extended beyond consumer electronics to encompass diverse fields, including medical applications like body temperature and heart rate monitoring. The rising demand for swift data monitoring via portable wireless devices has underscored the importance of energy-efficient components like LNAs. A thorough literature review will be used to analyze current trends in LNA requirements and designs, one of the many goals of the suggested research article. The study also seeks to identify the best LNA structure and parameters for particular application spectra or frequency bands.

Keywords: LNA, equilibrium, I/O identical, low energy expertise

1. Introduction:

The increasing prevalence of wireless standards and the emergence of dynamic applications such as software-defined radio are driving the need for the next generation of wireless devices. These devices aim to provide a multitude of services by integrating multiple standards into a single chipset. Reconfigurable multi-standard movable devices are clearly desirable because they provide the effective sharing and reuse of hardware components, which lowers the cost and physical footprint of the device. This research suggests a number of sophisticated circuit topologies that can satisfy several standards at a lower cost and are appropriate for applications using multiple standards.

This research paper proposal will center around three main ideas. It will first discuss the general issues that modern RF/wireless systems are encountering then look into solutions. This involves understanding the challenges of integrating multiple standards and finding ways to overcome these hurdles to ensure seamless functionality. Secondly, it will look at the challenges and design factors that come up while creating RF-CMOS integrated circuits. This includes analyzing the specific requirements for RF-CMOS technology, such as power efficiency, noise reduction, and integration density, and identifying strategies to address these challenges.

Finally, the paper will discuss key components essential to RF systems, specifically LNAs and RF Mixers. These components are crucial for the performance of wireless devices, as LNAs amplify weak signals with minimal added noise, and RF Mixers facilitate frequency conversion, a vital process in signal processing. By focusing on these aspects, the research aims to provide a comprehensive understanding of the requirements and innovations necessary for developing advanced multi-standard wireless devices.

To minimize power ingesting in wireless radio frequency (RF) systems, such as RF-Mixed-Signal System-On-Chip systems, one must have a thorough understanding of low-power plan at multiple

levels, including circuit blocks, sub-systems (such as transmitter, receiver, and PLL), and system levels. This work primarily focuses on optimizing power consumption for wireless RFICs.

One major difficulty facing wireless sensor nodes with tuner localization competences is lowering the cost of the localization function. Minimizing the cost of each wireless sensor node is critical because of the large amount that is frequently needed for different applications. Because conventional CMOS technology is especially well-suited for effective large-scale engineering procedures, it has the advantage of lower costs. Furthermore, the application of a methodical approach and thorough design can also result in a decrease in the costs related to a particular system. Simplifying and rationalizing the system building can save costs and energy consumption.

The proposed research will focus on several key areas. First, it will explore the optimization of power consumption at various levels, from individual components to the overall system. This includes investigating low-power design techniques and strategies for each part of the RF system, ensuring that the entire system operates efficiently. Second, the study will address the cost challenges associated with wireless sensor nodes by leveraging standard CMOS technology and proposing cost-effective design methodologies. By doing so, the research aims to make wireless localization more accessible and practical for large-scale applications.

Additionally, the paper will delve into the design and implementation of a pragmatic system architecture that balances performance, cost, and power consumption. This involves evaluating different architectural approaches and identifying the most effective solutions for minimizing energy usage while maintaining functionality. Through a comprehensive analysis and innovative design strategies, the research aims to contribute to the development of more efficient and cost-effective wireless RF systems and sensor nodes.

RF Receiver Chain and LNA Design Aspects

As shown in Figure 1, a down-conversion mixer is used after the LNA stage to convert the incoming RF sign to an IF. The original RF signal's incidence is higher than that of the IF. The DC level is where the frequency of the IF stage begins in direct conversion designs. By successfully isolating the RF stage from the IF stage, the use of separate incidences in the IF stage aids in achieving the necessary high gain and high constancy in RF receivers.

Improving the overall performance of RF receivers requires this isolation. In order to provide the following stages with a strong and clean signal, the LNA stage is in charge of amplifying weak RF signals with the least amount of additional noise. Once the signal is amplified, the down-conversion mixer translates the high-frequency RF signal to a lower IF, making it easier to process and analyze. The lower frequency of the IF stage allows for simpler and more efficient filtering and amplification, further improving signal quality.

In direct conversion receivers, starting the IF phase from the DC level eliminates the need for additional frequency translation stages, simplifying the design and reducing power consumption. This approach also minimizes the potential for signal distortion and interference, as the direct conversion process bypasses intermediate steps that could introduce noise or instability.

The separation of frequencies between the RF and IF stages ensures that the high-gain amplification needed for effective signal processing does not affect the stability of the RF stage. By isolating these stages, designers can optimize each one individually, achieving a balance between high performance and stability. This separation also facilitates the use of advanced filtering techniques in the IF stage, which can further enhance the overall presentation of the RF handset.

In summary, the use of a down-conversion mixer following the LNA stage, along with the strategic isolation of the RF and IF stages, is crucial for achieving high gain, high stability, and overall improved performance in RF receivers. This approach allows for more efficient signal processing, reduced power consumption, and minimized signal distortion, making it an essential design consideration in modern wireless communication systems.

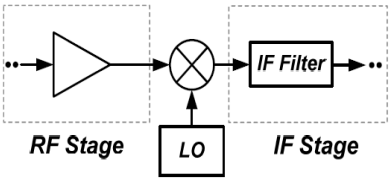

Figure 1: Block diagram of a mixer with an LNA and mixer in an RF architecture

The circuit for the BLE front-end receiver starts with the LNA. The five primary components that go into building an LNA are geometry, input matching networks, source degeneration feedback circuits, biasing circuits, and output matching networks. The circuit was constructed using the 45 nm processing technique derived from the GPDK. To ensure that an LNA is built correctly, one must have a solid understanding of RLC circuit theory principles and performance characteristics.

Higher degrees of integration seen in contemporary integrated circuits (ICs) enable the integration of more passive components, such as inductors, onto a single chip. The objectives pertaining to efficient RF, CMOS technology are more easily attained with this functionality. Additionally, the detrimental effects of transmission line effects—which were more pronounced in earlier technologies—are mitigated by employing contemporary design techniques with smaller device sizes. These features facilitate the process of overcoming the challenges associated with combining direct conversion receivers into a single integrated circuit.

Even with these improvements, there are still four main reasons why direct conversion receiver architecture is not widely used: I/Q incongruity, DC equipoises, flicker noise, and even order alteration. The design and implementation of RF circuits are significantly hampered by these ideas, which will be covered in-depth in this paper.

I/Q Mismatch: In direct conversion receivers, the in-phase (I) and quadrature (Q) components must be perfectly balanced to ensure accurate signal demodulation. Any mismatch between these components can result in image rejection problems, degrading the performance of the receiver.

DC Offsets: Direct conversion receivers often suffer from DC balances due to self-mixing of the local oscillator indication. This can create large DC components that interfere with the desired signal, necessitating complex DC offset cancellation techniques.

Flicker Sound: Also recognized as 1/f noise, flicker noise is particularly problematic at low frequencies and can significantly affect the performance of direct conversion receivers. Advanced design strategies are required to minimize this noise and improve the receiver's sensitivity.

Even Order Distortion: Even order distortion, including second harmonic distortion, can be particularly problematic in direct conversion receivers. It results from non-linearities in the circuit and can introduce unwanted signals that interfere with the desired operation of the receiver.

By addressing these factors, the research aims to provide solutions for integrating efficient and reliable straight adaptation receivers into single combined circuits, thereby advancing the capabilities of RF CMOS technology in modern wireless communication systems.

RFICs are the important mechanisms of wireless communiqué devices that are portable. Many people believe that CMOS technology is a very good way to construct RF front-ends because of a few important features, such as high degrees of integration, consistent device scaling, and affordability. The move towards the 5GHz band for working incidence is being driven by the growing customer demand for electronic services, which suggests that creative RF front-end solutions are required.

The LNA is very important in conventional design because it is a major factor in determining the system's overall sensitivity. The system must so adhere to a number of performance requirements. To properly suppress noise, the input resistance should stay constant at 50 ohms, the noise numeral should be reduced, and the gain of the other stages should be amplified.

MOSTs biased in the weak/moderate overturn zone are frequently used to minimize current noise levels. Reducing thermal noise is a crucial aspect of this biasing strategy in order to sustain high system sensitivity. Furthermore, 1/f noise is moved out of the signal band using chopper stabilization techniques, which guarantees good overall noise performance. These techniques are essential for maintaining the integrity of the signal and minimizing the impact of noise on the system.

The adoption of CMOS technology for RF front-ends in the 5GHz band is supported by its ability to integrate multiple functions onto a single chip, reducing both cost and physical size. This integration capability is crucial for meeting the growing demands for more advanced and efficient wireless communication devices. As the demand for electronic services continues to rise, innovative RF front-end designs that leverage CMOS technology will become increasingly important.

In summary, the LNA's role in RFIC design is pivotal due to its impact on system sensitivity and noise performance. By employing MOSTs in the weak/moderate inversion region and utilizing chopper stabilization techniques, designers can achieve the necessary performance metrics for modern wireless communication systems. The shift towards the 5GHz band underscores the need for continued innovation in RF front-end design, leveraging the strengths of CMOS technology to meet evolving consumer demands.

2. Literature Survey

Chang et al. (2020) have designed and implemented a low-power CMOS, LNA that operates within the 17.7-42.9 GHz frequency band. The future LNA is implemented on 65-nm CMOS technology and is intended for use in radio cosmic applications. This LNA, which is based on many strategies for data transmission enhancements, shows a notable sound figure and strong gain improvement over a wide incidence range with low power consumption. At the 3-dB level, there is a peak rise of 20.1 dB in data transmission volume between 17.7 and 42.9 GHz. The noise figure (NF) also varies from 2.8 to 4.3 dB. This method, which operates at a frequency of 28 GHz, generates an output power of 2. dBm at the 1 dB compression point (OP1dB), requiring less than 18 milliwatts of DC power. With a FOM value of 19 GHz/mW, the study emphasizes the position of distributed K-band and Ka-band LNAs. The chip's entire surface area, including the cushioning, is 0.45 mm^2.

An extensive research into the design and implementation of an LNA for a gatherer RF front-end utilized in narrowband remote infrastructures is given in a different paper by Amgothu Laxmi Divya et al. (2020). The remote receiver's main physical component is the LNA. The cascode CMOS LNA, designed exactly for reconfigurable requests like Wireless LAN, is the subject of this study. This study's main goal is to present an appropriate technique tailored for remote requests, while also highlighting the need for more exact execution strategies. The project's goal is to achieve significant amplification and noise reduction by using an inductive degeneration common-source stage. With a

full modeling approach, the suggested LNA yields a 2.44 GHz recurrence band. Reverse shielding and superior security measures are the keys to optimal input and output matching networks.

Both studies underscore the critical role of LNAs in enhancing the performance and efficiency of RF front-ends for various applications. Chang et al. (2020) demonstrate advancements in high-frequency applications with a broad operational range and minimal power consumption, making their LNA suitable for cosmic radio applications. In contrast, Amgothu Laxmi Divya et al. (2020) focus on narrowband, distant communication applications, emphasizing reconfigurability and precision in execution. Both studies contribute valuable insights into the design and implementation of LNAs, highlighting their importance in modern wireless communication systems.

Chang et al. (2021) developed the body drifting and self-inclination strategy, which offers a novel approach to low-power CMOS LNA design for sub-6 GHz 5G systems. This technique uses a resistor—set at 13.6 kΩ in this study—to establish a connection between the channel and the body of the semiconductor. The frequency range in which the suggested LNA operates is 3–9 GHz. Because of the onward body-to-source VBS, the LNA's forward transmission gain (S21) and NF are enhanced, lowering the threshold voltage (Vth) and reducing substrate leakage. With an NF of less than 3.5 dB, the CMOS LNA may now attain incredibly low power levels—some of the lowest ever logged for data broadcast above 6 GHz.

The work describes the self-inclination and body drifting phenomena in the 3-9 GHz CMOS LNA. The use of a small threshold voltage (Vth) in forward-biased VBS and the decrease in semiconductor substrate leakage are responsible for the development in the LNA's S21 and NF. Using low supply voltages (VDD) of 1 V or 0.8 V helps achieve low PD, which is important considering the low threshold voltage (Vth). Because of its low power dissipation and well-established performance metrics, the LNA is a great choice for usage in 5G networks that operate at incidences lower than 6 GHz. Among the noteworthy performance metrics are a PD of 3.3 mW and an NF of 2.89 dB. demonstrating the LNA's efficiency and effectiveness for modern tuner communiqué systems.

This approach highlights the significant advancements in LNA design for 5G applications, focusing on minimizing power consumption while maintaining high performance. The body drifting and self-inclination technique, along with forward-biased voltage biasing, provides a pathway for achieving these goals. The study by Chang et al. underscores the potential for CMOS technology to meet the demanding requirements of next-generation wireless networks through innovative design methodologies that enhance both performance and efficiency.

Sakshi Singh Dangi et al. (2021) used CMOS technology in their study to design an RFIC. In the business world, CMOS technology is being used more and more for Bluetooth, Wi-Fi LAN, and Worldwide Interoperability for Microwave Access (WiMAX) applications. When building RFICs, CMOS technology offers significant advantages in terms of cost and speed. Furthermore, a greater mark of downsizing on a single integrated circuit is made possible by CMOS technology.

Fundamentally, the goal of CMOS technology is to enable VLSI, or the efficient integration of several semiconductors into a single chip or substratum. This method offers RF designers a great deal of benefit since it makes CMOS technology operate more quickly. Because of the amazing levels of integration on a single chip, CMOS technology can function efficiently in the gigahertz frequency range, offering tremendous performance at a reasonable cost.

With the current state of virtual transmission infrastructures and the need for high signaling rates inside the most popular radio frequency sectors, the study emphasizes the viability of CMOS technology adoption. The decision to employ CMOS technology is straightforward due to its capacity for high performance, cost-effectiveness, and the ability to support advanced applications in

wireless communication systems. By leveraging the advantages of CMOS, RF designers can achieve significant enhancements in the speed and efficiency of RFICs, supporting the growing needs of modern communication technologies.

3. Methodology

The goal is to combine many standards into a single chip-set in order to minimize power consumption, maximize space usage, and improve the final product's competitive edge. The frequency spectrum for several standards is shown in Figure 3. Based on the evidence at hand, two separate conclusions can be drawn:

1. Meanings of "signal power" and "frequency bands" vary across dissimilar values: Different wireless standards may define signal power and frequency bands differently. This variation can pose challenges when integrating multiple standards into a single chip-set, as the chip-set must accommodate the requirements and specifications of each standard.

2. Numerous channels may access the hoarder with negligeable pre-separation, working as in-band obstacles and causing important distortion: In multi-standard wireless environments, multiple channels may operate within overlapping frequency bands. This can lead to interference and distortion, especially if there is minimal pre-separation between channels. Managing this interference and ensuring proper channel separation is crucial for maintaining signal integrity and system performance.

These conclusions highlight the complexities involved in integrating multiple wireless standards into a unified chip-set. Addressing variations in signal power definitions and frequency band allocations, as well as managing interference from overlapping channels, are key considerations in achieving successful integration and optimizing the performance of multi-standard wireless devices.

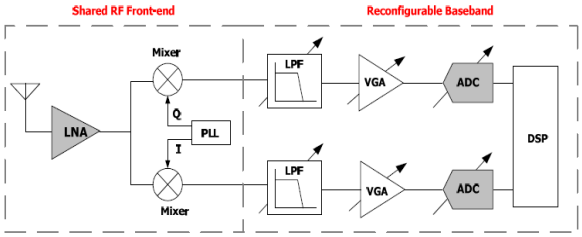

Figure 2. A decrease in conversion A block drawing of a reconfigurable direct change receiver based on a MIXER is shown.

Two major obstacles to the design of RF-down-conversion mixers can be distinguished from the data provided:

1. Interference of Signals in Close Range: Many users share a limited amount of frequency spectrum frequencies in wireless communication. Strong and weak signals may coexist in close proximity in this situation, making it difficult to reject interference and receive signals clearly. To solve this problem, RFIC radio receivers need to have both active and passive parts, which could be prone to flaws. These flaws may make it more difficult for the receiver to distinguish and select the intended signal from the wide range of other signs that are present in the spectrum.

2. Flaws in Receiver Design: The rejection of visual aids and the idea of range of motion are the two main issues that define the design of radio frequency receivers. The headset needs to be able to precisely pick the required signal and reject undesirable ones. It might be necessary to use bandpass filters with particular channel-width bandwidths and center frequencies that match the intended RF

signal in order to accomplish this goal. On the other hand, issues with signal processing and interference rejection may arise from flaws in the design of these filters and other receiver parts.

These challenges underscore the complexity involved in designing RF-down-conversion mixers for wireless communication systems. Addressing signal interference and imperfections in receiver design are critical considerations in optimizing the performance of RF receivers and ensuring reliable signal reception in multi-user environments.

The primary determinants of a receiver's dynamic range are the noise figure, the nonlinearity of the LNA, and the first mixer. The preselection RF bandpass filter may not be as effective at attenuating unwanted signals when there are strong interfering signals present together with the weak targeted RF signal. These massive interferers have the ability to overwhelm following IF circuits, making it more difficult for the receiver's front-end components—the mixer and LNA—to properly interpret the intended signal once it has been amplified. These interference sources also cause distortions in the receiver's SNR, which raises the input referred noise level.

Moreover, strong interfering signals might cause intermodulation distortions due to nonlinearities in the LNA and mixer, which could impact the desired channel during the downconversion process. These distortions have properties comparable to noise because the IF filter cannot distinguish amid unwanted signals and the essential IF signal.

A professional and technological strategy must be developed to solve these issues and meet the predetermined goals. This strategy will be covered in more part in the sections that follow. The wireless receiver architecture described in the previous unit for reconfigurable direct adaptation is shown in Figure 3. This architecture serves as the foundation for implementing strategies to mitigate the effects of interference and nonlinearities, thereby improving the dynamic range and overall recital of the receiver.

In instance, the LNA circuit's primary design objective can need the use of parallel narrowband receiver routes equipped with band selection switches. However, this method comes with extra costs, space requirements, and power usage. A highly linear broadband radio frequency front-end with swappable baseband blocks is a more adaptable and cost-effective solution to lower silicon size and power consumption. This approach allows the system to accomplish a number of goals while lowering the need for substantial hardware implementation.

Many circuit designs may need to be examined and simulated in order to get targeted designs with desired qualities like low power consumption and quick operational speed. Sturdy circuit simulator programs are necessary to achieve this goal. The following is a list of many tools that fit under this group:

1. SPICE: A widely used circuit simulator for analog and mixed-signal circuits, offering comprehensive analysis capabilities.

2. LTspice: A free, high-performance SPICE simulator developed by Linear Technology Corporation, now part of Analog Devices. It offers a user-friendly interface and powerful simulation capabilities.

3. Cadence Virtuoso: A comprehensive suite of design and simulation tools for analog, mixed-signal, and RF circuits. It provides advanced simulation capabilities and integration with layout design tools.

4. Keysight ADS: A powerful electric design mechanization software for RF, microwave, and high-speed digital requests. It offers advanced simulation and optimization features for RF circuit design.

5. Synopsys HSPICE: A gold standard SPICE simulator known for its accuracy and reliability in simulating complex analog and mixed-signal circuits. It provides extensive analysis capabilities and supports a wide range of semiconductor process technologies.

By utilizing these robust circuit simulator programs, designers can simulate and analyze various circuit designs to achieve targeted performance goals while minimizing power consumption and maximizing operational speed. These tools play a crucial role in the design and optimization of RF circuits, including LNAs, to meet the demanding requirements of modern wireless communiqué systems.

Simulator environment: SPICE (schematic level)

The HFSS (High-Frequency Structure Simulator) and SPICE software are industrialized by Keysight Technologies as part of their ADS.

1. HFSS: HFSS is an industry-leading electromagnetic simulation software used for high-frequency and high-speed electronic designs. It enables engineers to simulate and analyze the electromagnetic behavior of RF and microwave components, antennas, and integrated circuits. HFSS uses finite element method (FEM) technology to accurately predict electromagnetic fields, S-parameters, and other key parameters for complex structures. It is widely used in the design of RF and microwave tours, antennas, and systems for applications such as wireless communication, radar, and satellite communication.
2. SPICE: SPICE is a powerful simulation tool used for the analysis of analog and mixed-signal circuits. It provides accurate and detailed simulation of circuit behavior, including DC, AC, transient, and noise analysis. SPICE allows engineers to simulate numerous electronic mechanisms such as resistors, condensers, inductances, electronic transistor, and operative amplifiers. It is widely used in the design and verification of ICs, analog circuits, and mixed-signal circuits. SPICE imitations help engineers validate circuit performance, optimize designs, and identify potential issues before fabrication.

Both HFSS and SPICE are integral components of Keysight's ADS, a comprehensive EDA software suite used by engineers for the design, simulation, and optimization of RF, microwave, and high-speed digital circuits. ADS integrates various design and simulation tools, allowing engineers to seamlessly design and analyze complex electronic systems from concept to production.

Adoption of technology nodes:

The following goals are intended to be attained by the proposed research project:

To investigate present trends and examines on LNA requirements and projects, conduct a thorough analysis of the literature.

Determine the LNA's final analysis situs and stipulations for the selected request band (spectrum).

Complete the circuit topology according to the request and the chosen semiconductor expertise (RF-CMOS at 65 nm or 130 nm, in this case).

Assemble and simulate the LNA's behavior in an actual radio environment.

Verify and modify the design to comply with the requirements, then publish the results—both conventional and novel—in reputable journals.

The topic of conversation is CMOS technology, specifically how it applies to and is relevant for people who are at or above Level 49. Additionally, the semiconductor technology choices for the low voltage node are either 130 nm or 180 nm. These specifications provide a framework for conducting research and developing a Low Noise Amplifier tailored to specific application requirements and semiconductor technologies.

The proposed investigate project aims to achieve the following objectives:
1. Conduct a thorough analysis of the literature to evaluate the most recent advancements and requirements in the LNA domain.
2. Decide on the final topology and specifications for the band (spectrum) that the LNA application will use.
3. Select the schematic topology based on the requirements of the specific application and technology (e.g., 65 nm or 130 nm RF-CMOS).
4. Construct a thoughtful and well-thought-out LNA plan within an actual radio setting.
5. Check that the design complies with the standards and make necessary adjustments. Then, share the new and proven findings that have been published in credible academic journals.
These objectives outline the systematic approach to conducting research on low-noise amplifiers, from literature analysis to design implementation and verification, with the ultimate goal of contributing valuable insights to the field and advancing the state of the art in RF technology.

4. Findings and Conversation

Stabilization components added to an amplifier

The utilization of a chopper technique serves to enhance the performance of the amplifier and mitigate the presence of offset and flicker noise. Additionally, a ripple reduction loop (RRL) is implemented to counteract the effects of ripple resulting from the up-modulation of offset and flicker noise. By employing a multi-path architecture consisting of both a low-frequency path (LFP) and a high-frequency path (HFP), the overall transfer function of the RRL operation can be adjusted to eliminate notches.

In the low-frequency path amplifier, a Regenerative Receiver with Limiter (RRL) and chopper technique are utilized. Conversely, a class-AB output stage is employed in the high-frequency path amplifier to enhance power efficiency. The resulting frequency response of the system is first-order, effectively compensated for by layered Miller compensation of the transfer functions of the low-frequency path (LFP) and high-frequency path (HFP).

Fabricated using a 0.18 μm 1P6M complementary metal-oxide-semiconductor (CMOS) technology, the suggested low-noise functional amplifier occupies an operational area of 1.18 square millimeters and consumes 0.174 milliwatts of power at 1.8 volts. The amplifier exhibits an input mentioned noise level of 11.8 nV/Hz, a UGBW of 3.16 MHz, and a NEF of 4.46.

With the outside basis resistance set to 50 Ohms and a matching network linked to the input, the couple of S22 can be assumed to represent the ideal load echo coefficient, provided that the input similar network remains constant. This configuration ensures efficient power transfer and optimal performance of the amplifier in practical applications.

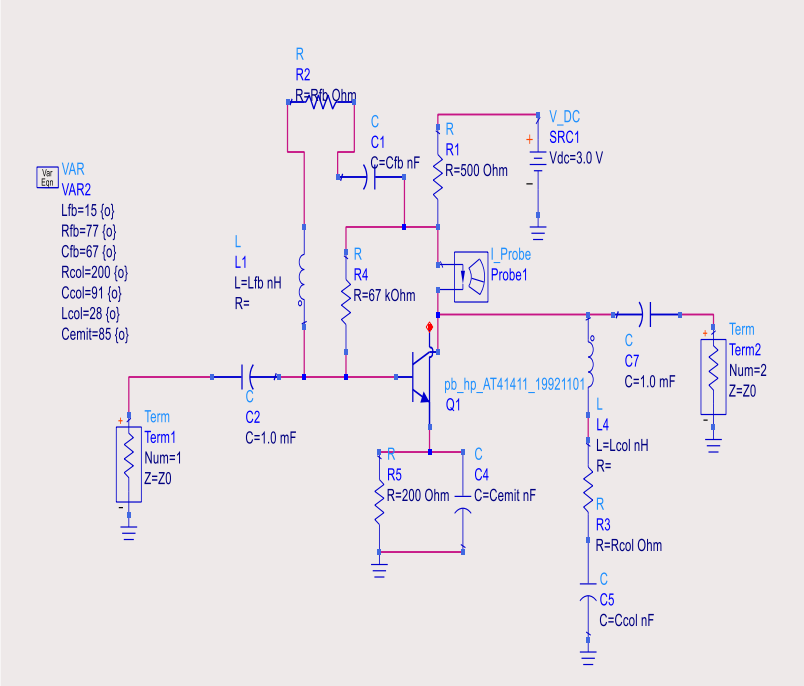

Figure 3: Amplifier with stabilization components

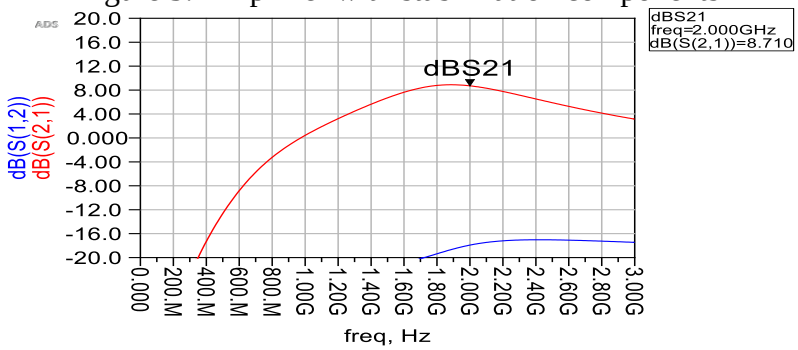

Figure 4: Regularity reply of amplifier gain

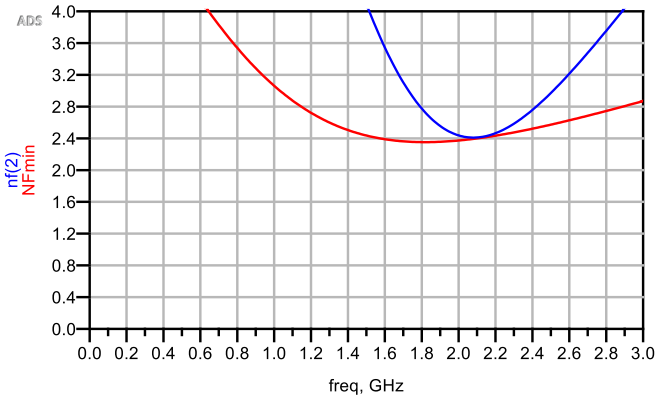

Figure 5: Noise efficacy factor retort

Z_Load
154.303 + j31...

Gain, input match, output match, and noise figure are all optimized for amplifier input and output matching networks.

Many LNA circuits implemented in RF CMOS technology have been established in previous research; nevertheless, the literature currently in publication lacks thorough design approaches that are explicitly targeted at very low noise values. In many cases where linearity is prioritized over noise figure, a compromise between the two often results in a partial sacrifice of noise performance. Nevertheless, achieving robust linearity and noise performance is feasible, a topic that will be explored in greater detail in subsequent sections of this study.

The LNA has a major impact on the total noise figure, and gain and power dissipation settings are the main areas where receiver noise performance is optimized. Through the use of interactive and simulation methodologies, other properties are modified throughout the design phase to satisfy the unique needs of diverse applications. These techniques enable engineers to fine-tune the LNA's parameters and characteristics to achieve the desired noise performance while ensuring compatibility with the application's requirements.

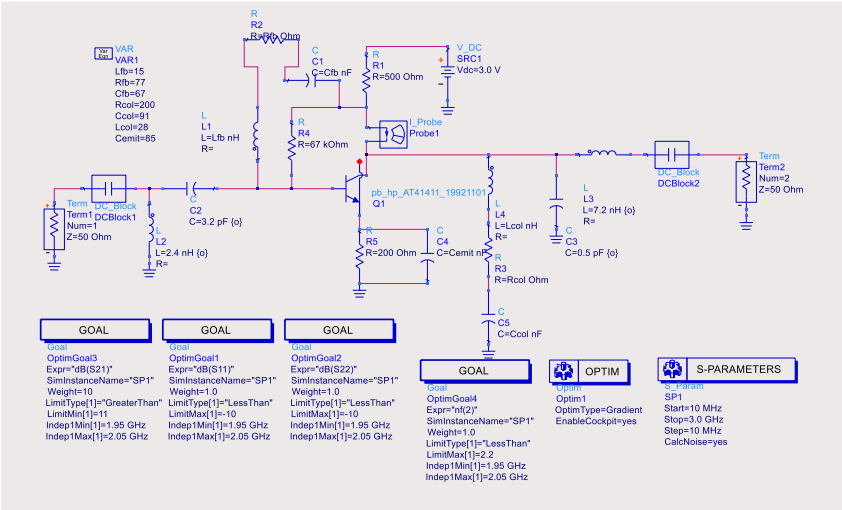

Figure 6: Amplifier with effort and yield identical networks

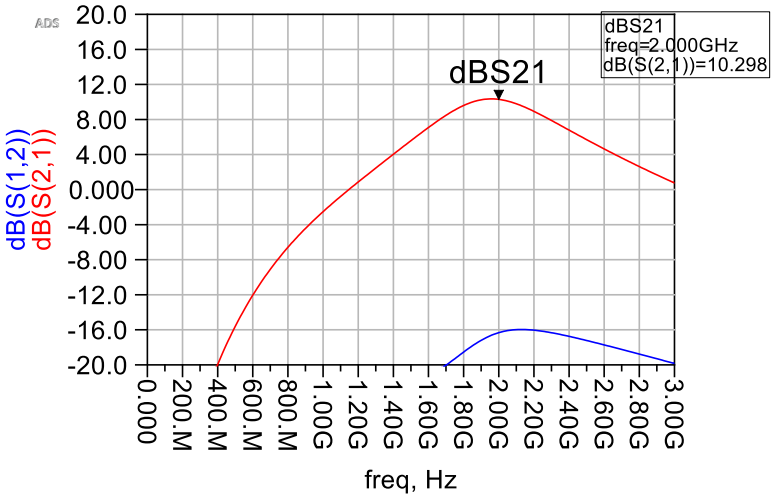

Figure 7: An amplifier's incidence response when its input and output networks are the same

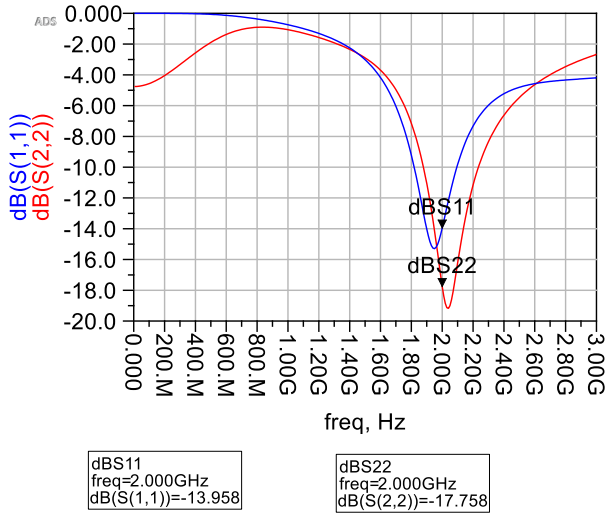

Fig 8: Equilibrium, comparable input and output components added to the amplifier

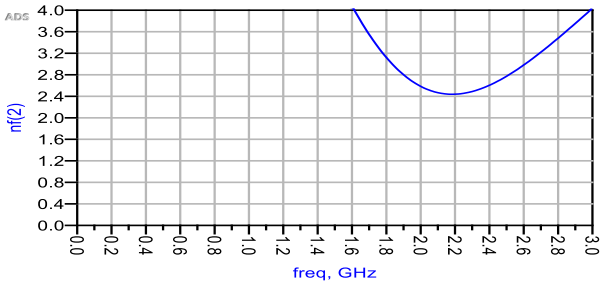

Figure 9: Reuniting the amplifier's noise efficacy factor with the same input and output networks

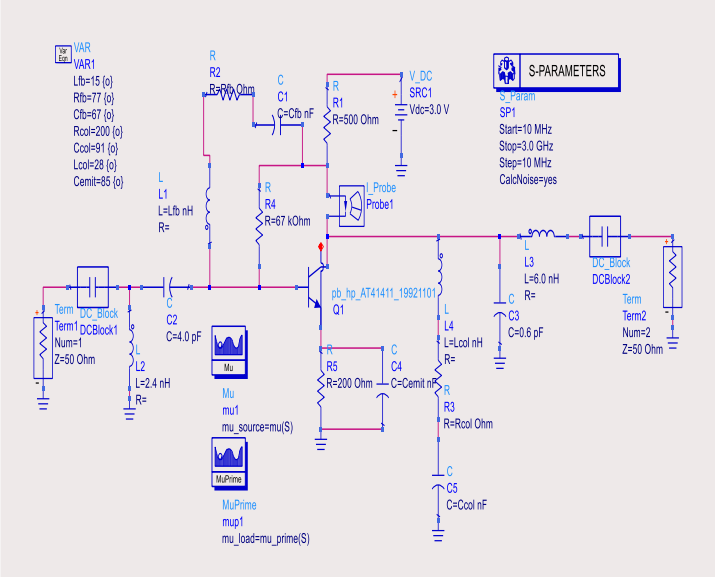

Figure 10: Equilibrium, input, and output identical components added to the amplifier

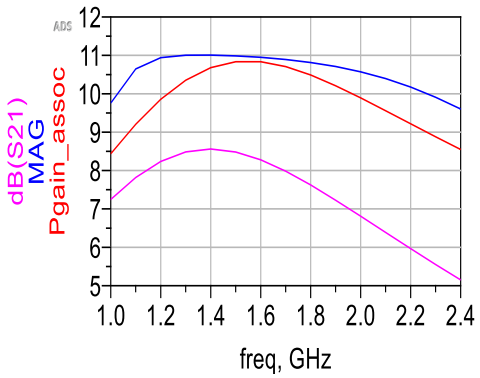

Figure 11: Amplifier frequency return with stabilization, comparable input and output components added

In the analysis of low-noise amplifiers (LNAs), key parameters under scrutiny include the maximum achievable gain, equivalent power gain when input and output are conjugately matched for minimal noise figure, and the value of dB (S21). By employing Z0 Ohm terminations, optimal conditions can be established to determine both the minimal noise figure and noise figure of the LNA. These terminations facilitate the conjugate matching of input and output, reducing reflections and optimizing noise performance. The maximum achievable gain denotes the highest amplification capability of the LNA, crucial for ensuring adequate signal amplification while keeping noise levels low. The equivalent power gain showcases the LNA's ability to amplify signals with minimal added noise under ideal conditions. Meanwhile, dB (S21) quantifies the signal gain in decibels, providing insight into the LNA's performance characteristics. Achieving low noise figure values is essential for preserving signal integrity and maximizing receiver sensitivity.

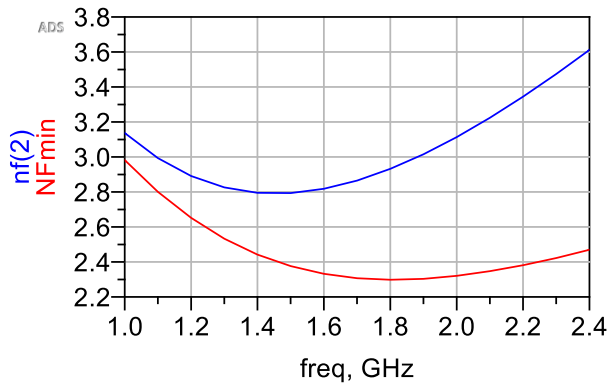

Figure 12: Return of the amplifier's noise efficiency factor after stabilization, input, and output components were added.

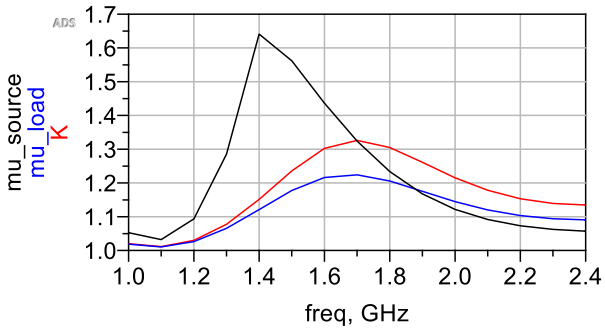

Figure 13: K Geometric stability factor, mu_load, smu_source, and firmness factor

5. Conclusion:

The construction of LNAs often involves the utilization of SiGe (BiCMOS) and CMOS transistors, a trend reflected in various research articles. However, commercially available LNAs commonly employ GaAs-pHEMT technology. It's noteworthy that only a limited number of commercially available LNAs boast a noise symbol below 0.5 dB. Comparing silicon processes to other transistor technologies, the former provides more integration. Due to their remarkable presentation, GaAs-HEMT and other BiCMOS technologies, most notably SiGe, have historically conquered the RF industry. Still, CMOS technology is becoming more and more popular. It is clear that there is a trade-off between power, gain, linearity, and noise figure. It is feasible to create an LNA system with a low noise figure and desired linearity qualities by sacrificing power, gain, and other parameters. The particular function or application determines the criteria for LNA design. Base stations prioritize attaining favorable linearity qualities and a low NF, whereas other applications such as WLAN, Bluetooth, GPS, and others prioritize linearity and a satisfactory noise figure.

6. Acknowledgement:

All authors would like to thank Integral University, Lucknow for providing the manuscript number **IU/R&D/2023-MCN0002292** for the present research work

References:

[1] M. Lundstrom, “Moore's law forever?”, Science, Vol. 299, No. 5604, pp. 210-211, Jan. 2003.
[2] P. Darling, “Intel to invest more than $5 billion to build new factory in Arizona”, Intel Pressroom, 18. Feb. 2011.

[3]. I. A. W. Vance, “An integrated circuit VHF radio receiver,” The Radio and ElectronicEngineer, vol. 50, no. 4, pp. 158-164, 1980.
[4]. J. F. Wilson, R. Youell, T. H. Richards, G. Luff and R. Pilaski, “A single-chip VHFand UHF receiver for radio paging,” IEEE Journal of Solid State Circuits, vol. 26, pp.1944-1950, December 1991.
[5]. R. C. French, “A high technology VHF radio paging receiver,” in International Conferenceon Mobile Radio System and Technique, York, UK, pp. 11-15, 1984.
[6]. K. Nagata, M. Akahori, T. Mori and S. Umetsu, “Digital display radio paging system,”in NEC Rec. &Devel. no. 68, pp. 16-23, January 1983.
[7]. K. Nagata, D. Ishii, T. Mori, T. Oyagi and T. Seo, “Slim digital pagers” in NEC Rec.&Devel. no. 74, pp. 55-64, July 1984.
[8]. K. Yamasaki, S. Yoshizawa, Y. Minami, T. Asai, Y. Nakano and M. Kuroda, “Compactsize numeric display pager with new receiving system,” in NEC Rec. & Develop.,vol. 33, no. 1, pp. 73-81, January 1992.
[9]. A. Burt, “Direct conversion receivers come of age in the paging world,” in GECRev., vol. 7, no. 3, pp. 156-160, 1992.
[10]. S. Tanaka, A. Nakajima, J. Nakagawa and A. Nakagoshi, “High-frequency, low-voltagecircuit technology for VHF paging receiver,” IEICE Trans. Fundamentals of Electronics,Communication and Computer Science, vol. E76-A, no.2, pp. 156-163, 1993.
[11]. A. Mashhour, W. Domino and N. Beamish, “On the direct conversion receiver’ atutorial,” Microwave Journal, pp. 114-128, June 2001.
[12] Jin-Fa Chang, et .al., “3-9 GHz CMOS LNA Using Body Floating and Self-Bias Technique for Sub-6 GHz 5G Communications”, IEEE 2021.
[13] Sakshi Singh Dangi et. al., “A Review on Lna Design For Wi -Max Applications”, International Research Journal of Modernization in Engineering Technology and Science, Volume:03/Issue:09/September-2021.
[14] Mahesh Mudavath et. al., “Design of Cryogenic CMOS LNAs for Space Communications”, Journal of Physics, ICCIEA 2020.
[15] Rajani Bisht and S. Qureshi, “Design of Low-Power Reconfigurable Low-Noise Amplifier with Enhanced Linearity”, IEEE 2019.
[16] Roman Yu. Musenov et. al., “The S- and C- band Low-power CMOS LNA Using the Current-reuse Technique”, IEEE 2021.
[17] L. Belostotski and J. W. Haslett, “Noise figure optimization of inductively degeneratedCMOS LNAs with integrated gate inductors,” IEEE Transactions on Circuits andSystems-I: Regular Paper, vol. 53, no. 7, 2006.
[18] J. S. Goo, H. T. Ahn, D. J. Ladwig, Z. Yu, T. H. Lee and R. Dutton, “A noise optimizationtechnique for integrated low-noise amplifiers,” IEEE Journal of Solid-State Circuits,vol. 37, no. 8, pp. 994- 1002, August 2002.
[19] B. Razavi, “Architectures and circuits for RF CMOS receivers,” IEEE Custom IntegratedCircuits Conference, pp. 393- 400, May 1998.
[20] Deepak Balodi, ArunimaVerma and PA Govidacharyulu, “A high gain low noise amplifier design & comparative analysis with other MOS-topologies for Bluetooth applications at 130nm CMOS,” 2016 IEEE Industrial Electronics and Applications Conference (IEACon), IEEE Xplore, pp 378-383, 2016.
[21] R. Salmeh, “A low voltage / low power 1.5 GHz low noise amplifier,” IEEE SarnoffSymposium on Advances in Wired and Wireless Communications, pp. 81-84, April 2005.
[22] AmgothuLaxmi Divya1, Mahesh Mudavath, Ch S Ranadheer, Mohamed Afzal andR.Venkateswarlu, “Low Noise Amplifier Design and Performance Analysis of RFFront-End for Narrow Band Receivers,” Journal of Physics: Conference Series, IOP Publishing, ICCIEA 2020.
[23] AayushAneja et. al., “Design and analysis of a 1.1 and 2.4 GHz concurrent dual-band low noise amplifier for multiband radios”, AEU - International Journal of Electronics and Communications, Volume 134, May 2021, 153654.
[24] H. -H. Chen, W. -C. Cheng, C. -H. Hsieh and Z. -M. Tsai, "Design and Analysis of High-Gain and Compact Single-Input Differential-Output Low Noise Amplifier for 5G Applications," in IEEE Microwave and Wireless Components Letters, vol. 32, no. 6, pp. 535-538, June 2022, doi: 10.1109/LMWC.2022.3149033.
[25] Roobert, A.A., Rani, D.G.N. Design and analysis of a sleep and wake-up CMOS low noise amplifier for 5G applications. Telecommun Syst 76, 461–470 (2021). https://doi.org/10.1007/s11235-020-00729-y.

[26] Amir Hossein Kazemi, Mohsen Hayati, “Design and analysis of a flat gain and linear low noise amplifier using modified current reused structure with feedforward structure”, Integration, Volume 81, 2021, Pages 123-136, ISSN 0167-9260, https://doi.org/10.1016/j.vlsi.2021.05.013.

[27] Ahmer, Mohd, N. R. Kidwai, and M. Yusuf Yasin. "Memristor emulation and analog application using differential difference current conveyor of CC-II in CMOS technology." Materials Today: Proceedings 51 (2022): 234-239.

[28] Ahmer, Mohd, N. R. Kidwai, and M. Yusuf Yasin. "A novel memristor emulator design and universal biquad filter application using second generation high swing differential current conveyor transconductance amplifier in 130 nm CMOS process." Materials Today: Proceedings 51 (2022): 150-155.

[29] Chaturvedi, Sumita, Prem Kumar Bharti, and Syed Nadeem Akhtar. "Metal-on-Metal hip prostheses lubrication analysis for Newtonian elastohydrodynamic fluid." Materials Today: Proceedings 46 (2021): 6859-6866.

[30] Saraswat, Kirti, T. Usmani, and Savita Maurya. "GaAs solar cell performance improvement by design optimization using NSGA approach." Materials Today: Proceedings 51 (2022): 178-185.